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# Selector-Less Resistive Random Access Memory (RRAM) with Intrinsic Nonlinearity for Crossbar Array Applications

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# Selector-Less Resistive Random Access Memory (RRAM) with Intrinsic Nonlinearity for Crossbar Array Applications

**by**

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# Abstract

## Selector-Less Resistive Random Access Memory (RRAM) with Intrinsic Nonlinearity for Crossbar Array Applications

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With increasing demand for high-density memory applications, alternative memory technology has been intensively investigated for replacing conventional charge-based flash memory. Among the emerging memory technology, resistive random-access memory (RRAM) device holds great potential as an emerging candidate because of its simple design, high-speed operation, excellent scalability and low power consumption. However, the sneak path current ($I_{sneak}$) through unselected neighboring cells is a major problem in crossbar RRAM array configuration, which significantly affects the read operation and accuracy. To address the sneak path current issue, a transistor or a selector device is typically integrated with the memory device i.e. 1T-1R and 1S-1R configurations. Unfortunately, integrating an additional selector device considerably increases the manufacturing complexity and cost. In this work, the selectorless 1R-only RRAM with self-rectifying behavior i.e. nonlinearity are proposed for suppressing the sneak path current without utilizing transistors or selector devices. Bilayer structures i.e. high-k layer/low-k layer stacks are highly scalable, while suppressing the sneak path currents in crossbar RRAM array. The nonlinearity (NL) modulation is also investigated

by different operating schemes. The nonlinearity with calculated array size (N=120) utilizing the bilayer selectorless RRAM devices has been demonstrated. In addition, the nonlinearity can be modulated by utilizing various operation schemes, i.e. SET compliance current limit, positive pulse modulation, V-sweep, and I-sweep etc. The numerical read margin calculation of selectorless RRAM for crossbar array applications, device area effect, device thickness effect, and various operation schemes for good energy efficiency are also discussed. The result presents comprehensive insights into development and optimization of bilayer selectorless RRAMs with high nonlinearity (~120), good memory window (~$10^2$), and low switching energy (~40 pJ/bit), which enable the high- density storage, low-power crossbar array memory applications.

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# Chapter 1: Introduction

## 1.1 NON-VOLATILE MEMORY

The floating gate (FG) nonvolatile memory has been the main structure of nonvolatile memory devices, since its invention in 1967 by D. Kahng and S. M. Sze. The non-volatile memory has been widely utilized in the portable electronic products such as mobile phones, digital cameras, notebook computers, and USB flash drives. The typical structure of a nonvolatile flash memory device is shown in Figure 1.1. The operating principle of conventional nonvolatile memory is based on the use of polycrystalline silicon as a floating gate to store charges injected from a channel[1]. Once charges are present in the floating gate, the threshold voltage of the memory device will be changed. The logical signals "0" and "1" are thereby defined by the levels of threshold voltage. However, as device size shrinks, the typical flash memory device will continue to suffer from reliability issues e.g. retention and endurance. As the typical flash memory device scales down to the nanoscale, stored charges in the floating gate can easily tunnel through the tunnel oxide to the Si substrate[2]. The reason for this is that the thickness of the scaled tunnel oxide cannot provide enough blocking effect to keep the stored charges. Additionally, the leakage paths created in the tunneling oxide after thousands of operations, which results in a rapid and complete loss of stored charges.

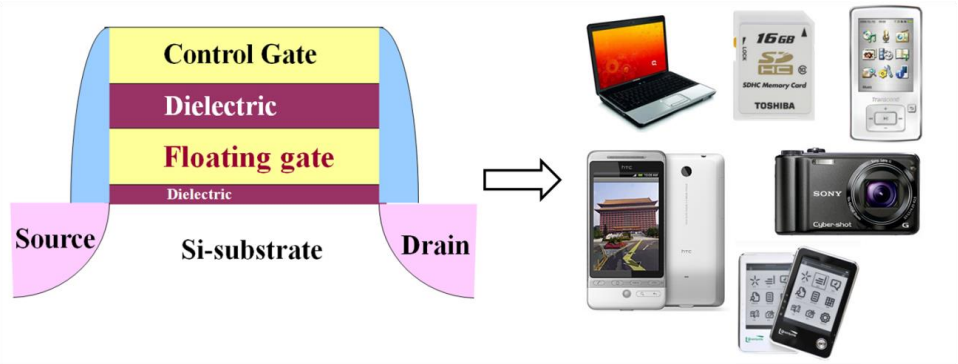



Figure. 1.1. Device structure of conventional nonvolatile flash memory and its application on electronics products

In order to solve the above-mentioned problems, researchers have presented methods which change the storage layer without changing the device structure, such as utilizing the silicon nitride (served as a trapping layer in SONOS (silicon/oxide/nitride/oxide/silicon)) [3-6] or discrete nanocrystals [7-11] employed as storage cells. The stored charges can exist in the trap states of the charge trapping layer in the distributed nanocrystals to maintain the information, even if localized leakage paths are present in the tunneling oxide. However, making changes to the storage layer still cannot solve issues of scale-down and program/erase speed. Therefore, researchers have considered new storage layers and novel structures in nonvolatile memory devices to substitute the conventional floating gate device. The new nonvolatile memory devices must exhibit better program/erase speed, retention, endurance and lower power consumption. As for the scale-down requirements towards some specific applications, the new device should also be compatible with cross-point structures.

Therefore, a great deal of potential memory structures have been proposed, with some transferring into a production line, such as phase change memory (PCM)[12], magnetic random access memory (MRAM)[13] and ferroelectric random access memory (FeRAM)[14]. In the innovation of memory devices, resistance random access memories

(ReRAMs) have gained significant research interest as an alternative for next-generation nonvolatile memory[15-20] due to its high density, low cost, low power consumption, fast switching speed and simple cell structure. In addition, ReRAMs can possess program/erase speeds as high as SRAM, density as high as DRAM and nonvolatility for flash memory; therefore, ReRAMs demonstrate an extremely high potential for replacing NAND flash and DRAM to become the next-generation nonvolatile memory.

### 1.2 RESISTIVE RANDOM ACCESS MEMORY (RRAM)

In recent years, memory technology including static random access memory (SRAM), dynamic random access memory (DRAM), and flash memory are encountering challenges due to the continued scaling down of the designs. The ReRAM device structure is composed of a sandwiched metal/insulator/metal (MIM) layers. By applying voltage or current, the resistance of the device can be changed, thereby giving the device data storage characteristics. ReRAM first originated from Hickmott in the 1960s; he discovered that the resistance of $AlO_x$ could be modified after voltage or current operation. In recent years, the resistive switching behaviors of a large variety of materials have been reported, including binary metal oxides such as NiO, CuO and $HfO_x$. The electroformation process is usually required and the percolation path formed after soft breakdown process. The logic state “0” or “1” is defined by different resistance values i.e. high resistance state (HRS) oR low resistance state (LRS), and can be read by applying a relative lower voltage to measure the resistance state (Figure 1.2). ReRAM devices exhibit good nonvolatile characteristics, and the stored data can be retained until the next data is written. Unlike conventional flash memory, ReRAM uses resistance value to define the data state, and because its resistance state can be retained for a long time, ReRAM has better data storage capability (including switching speed, switching energy,

and operation voltage)[21-23].Characteristics such as low operation voltage, a fast program/erase speed and good scale-down capability make ReRAM a suitable candidate for the next-generation of nonvolatile memory. Hence, ReRAM is gaining significant interest in academia and industries for its high practicality and potential for commercial applications.

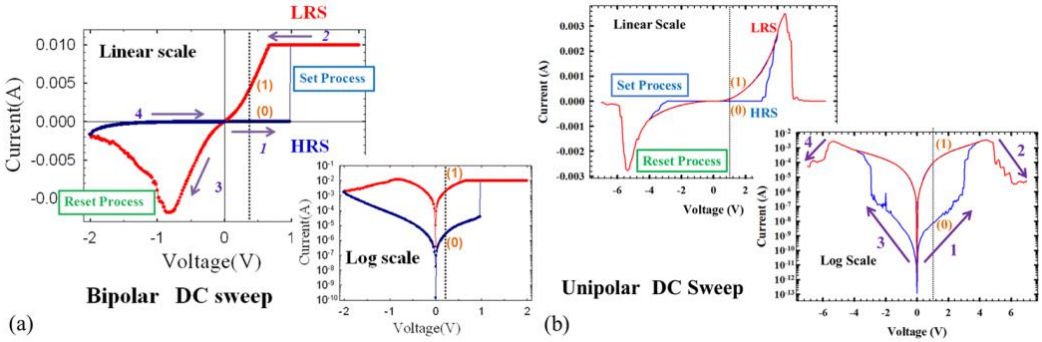



Figure. 1.2. Switching characteristics of ReRAM device (a) bipolar-type and (b) unipolar-type of $SiO_x$-based ReRAM.

### 1.3 OXIDE-BASED SELECTOR-LESS RESISTIVE RANDOM ACCESS MEMORY (RRAM)

Among several types of next generation memory devices, resistive random access memory (RRAM) composed of a simple metal-insulator-metal (MIM) structure has increasingly been attracting much attention as a promising candidate for next-generation nonvolatile emerging memory according to its potentially ultra-high density production probability, faster switching speed (<10 ns), compatibility with a crossbar structure with CMOS integration, lower energy consumption, high-density storage , and the feasibility for neuromorphic computing architecture design (Figure 1.3).

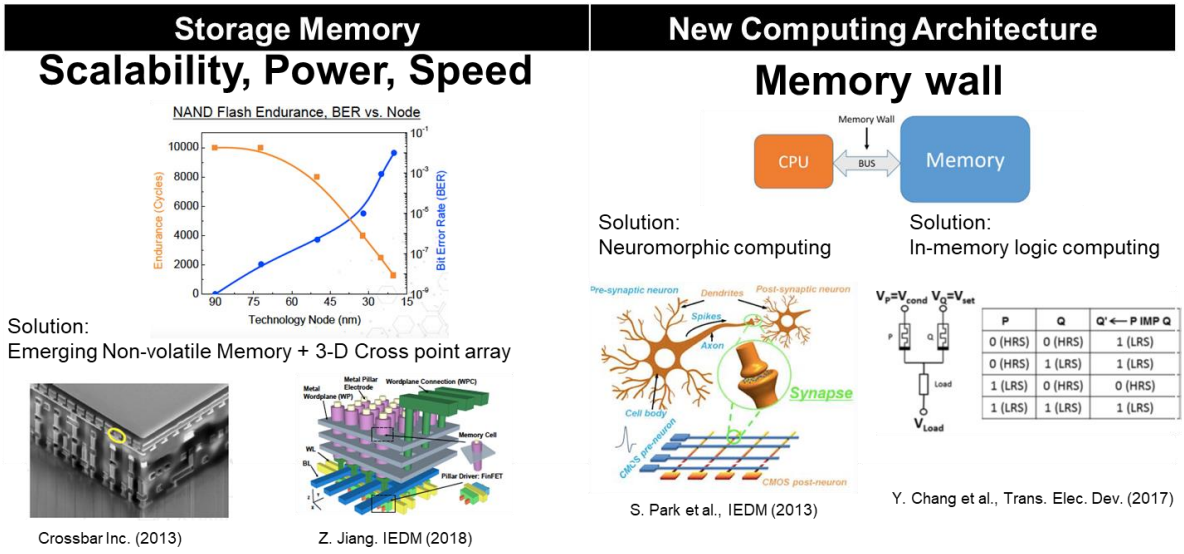



Figure. 1.3. Device structure of conventional nonvolatile flash memory and its application on electronics products

Table 1.1. Comparison of the current prototypical and emerging memory

| | DRAM | STTRAM | PCM/ 1T1R RRAM | Cross point RRAM | NAND |
|---|---|---|---|---|---|
| Read Latency | 20ns | ~ 50ns | ~100ns-200ns | ~100ns-200ns | ~10us |
| Write Latency | 20ns | ~ 50ns | ~1us | ~1us | ~10us |
| Read Endurance | >1e15 | $>10^{11}$ | $>10^{7}$ | $>10^{7}$ | $>10^{7}$ |
| Write Endurance | >1e15 | $>10^{11}$ | $>10^{6}$ | $>10^{6}$ | 2K-100K |
| Write/Read Energy/bit | <10pJ/bit | ~25pJ/bit | ~100-200 pJ/bit | ~100-200 pJ/bit | > 100pJ/bit |

With increasing demand for high-density memory applications, alternative memory technology has been intensively investigated for replacing conventional charge-based flash memory. Among them, resistive random access memory device holds great potential as an emerging candidate because of its simple design, high-speed operation, excellent scalability, and low power consumption (Table 1.1)[24-28]. However, the sneak-path current through unselected neighboring cells is a major problem occurring in crossbar RRAM configuration, especially for large memory arrays. This in turn

significantly affects the read operation. To address the sneak path current issue, a selector device (or a threshold switch) integrated with a memory device has been developed. Several bidirectional selector devices have been proposed for bipolar RRAM, such as transistor device, tunneling diode, Schottky diode, and threshold switches.[29-31] Unfortunately, these additional selector devices i.e. 1S-1R configuration considerably increase the process complexity and cost. Therefore, a selectorless memory i.e. 1R-only RRAM with nonlinear characteristics and high scalability is desirable (Fig. 1(a)). The built-in nonlinearity (NL) can alleviate the sneak current because the on-state of the selected cell can be read at a "high-voltage" region, while the sharp conductance drop at "low-voltage region" effectively suppresses sneak current through unselected cells (e.g. V/2 and V/3 read schemes). The nonlinearity is defined as the current at high voltage i.e. $V_{read}$, divided by the current at low voltage i.e. 1/3 Vread in V/3 read scheme, and 1/2 $V_{read}$ in V/2 read scheme. In other words, the sneak current can be avoided by taking advantage of nonlinearity in the self-rectifying I-V characteristics i.e. low resistance state (LRS) of 1R selectorless RRAM itself. Several approaches (e.g. nanocrystals,[32] active layer thickness engineering[33] etc.) and material systems (e.g. $TiO_x$,[33-34] $Ta_2O_5$,[35-36] $Pr_{0.7}Ca_{0.3}MnO_3$[37-38]etc.) have been proposed to improve NL of a single RRAM device. Among them, selectorless RRAMs utilized by multilayer stacking engineer i.e. oxide stacks have been widely reported (e.g. $Ta_2O_5/TiO_x$[39], $Al_2O_3/TiO_x$[40], $TaO_x/HfO_x$[41]etc.). Recently, nonlinear behaviors by using oxide stacks have been reported (i.e. in I-V characteristics) with various proposed mechanisms, such as different oxygen concentration between top/bottom layer[39, 42], phase change material integration[41], electrical resistor[43], Schottky barrier between two layers[44], charge transport mechanism exchange (i.e. space charge limit current to F-N tunneling[45-46]), different tunneling barrier of filament/bilayer interface[47], different filament widths[48], etc.

First, the electrical characteristics of conventional oxide-based RRAM (e.g. $HfO_x$ and $SiO_x$) have been investigated comprehensively, and filamentary structures were observed through material analysis methods. Second, the use of bilayer structures i.e. $HfO_x/SiO_x$, has been proposed by inserting a low-k layer (e.g. $SiO_x$) and programmed (SET) low resistance state (LRS) under compliance current limits (CCL) i.e. gap design method, so that the nonlinearity in selectorless RRAM is enhanced[49-50]. Third, carbon-based materials attract considerable interests for RRAM devices due to its environmental sustainable manufacturability, and high mechanical flexibility for soft electronics applications. Among them, the potentials for using graphite-based materials e.g. graphite and graphite oxide to deliver high performance of bipolar resistive switching memories have been studied on flexible, transparent and rigid substrates i.e. Pt/GO/Ti/Pt[51], Cu/a-C/Al[52], Al/GO/ITO[53] etc. However, the built-in nonlinear nature of graphite-based RRAM devices with stable RS operations has not yet been investigated. In this work, the nonlinearity in bilayer graphite-based RRAM devices has been also demonstrated by controlling the SET CCL i.e. optimizing the nonlinearity to efficiently suppress sneak path current. In addition, the nonlinearity is tunable and can be enhanced by optimized voltage pulse scheme, which is significantly useful in controlling device variability and reliability. Finally, built-in nonlinearity is demonstrated in 1R-only selectorless RRAM for the low-power memory array, high-density storage, and in-memory neuromorphic computational configurations applications.

### 1.4 DISSERTATION ORGANIZATION

This research work is organized as following:

In Chapter 1, the oxide-based filamentaryselectorless RRAM is introduced with the typical electrical characteristics and potential mechanisms. Chapter 2 covers dynamic

conductance characteristics in $HfO_x$-based resistive random access memory. Chapters 3 and 4 covers two types of high-k/low-k bilayer selectorless RRAM with intrinsic nonlinearity for suppressing the sneak path current in the array application. In Chapter 3, the $HfO_x/SiO_x$ bilayer selectorless RRAM is presented with the internal filament modulation through the SET compliance current limit (CCL) i.e. low-k switching gap design method. In Chapter 4, the graphite-based selectorless RRAM is demonstrated with improved nonlinearity and the tunable nonlinearity for tail-bits by utilizaing pulse schemes. Chapter 5 covers the relaxation characteristics and resistive switching identification methodology in $HfO_x/SiO_x$ bilayer devices. In Chapter 6, the numerical read margin calculation and experimental results of selectorless RRAM in crossbar array configuration are discussed. Finally, a summary of works performed and the proposed future work plan will be discussed.

# Chapter 2: Dynamic Conductance Characteristics in $HfO_x$-based Resistive Random Access Memory

## 2.1 INTRODUCTION

Resistive random access memory (RRAM) has attracted a great deal of attention as a potential candidate for next-generation emerging memory owing to its high switching speed, excellent scalability, low-voltage operation and multilevel storage[24-25,54-55]. There have been many studies of binary metal oxides such as $FeO_x$, $ZrO_x$, $TiO_2$, NiO, $Al_2O_3$, $Cu_xO$, and $HfO_x$[56-61, 20]. These metal-insulator-metal structures exhibit resistance switching characteristics in part due to the inevitable existence of non-stoichiometry in insulating thin film. Among these insulators, hafnium oxide ($HfO_x$) was proposed as the most promising material system based on the 2015 International Technology Roadmap for Semiconductors (ITRS) due to its overall performances on the reliability including endurance property (>$10^{12}$ cycles), retention (>10 years at 85 $^oC$), and operation stability (i.e. current limiting operation) conformed with the requirements of non-volatile memory and storage class memory applications[62]. Furthermore, $HfO_x$ has been extensively studied and used as the gate dielectrics for MOSFETs since 45 nm technology node and is obviously compatible with the complementary metal–oxide–semiconductor (CMOS) process. In this work, a dynamic conductance method, i.e. derivative of DC I-V response ($\partial I/\partial V$), has been used to study the $HfO_x$-based RRAM characteristics in Al/$HfO_x$/Al and Al/$AlO_x$/$HfO_x$/Al structures. $HfO_x$-based devices have been reported exhibiting good switching properties in different operating polarities in four quadrants[63]. This dynamic conductance method can be used to study the RESET behaviors in bipolar switching as well as in unipolar switching. Analyzing the dynamic conductance can help understanding the RESET behaviors (e.g. one-step-like and multi-step-like) and filament

degradation characteristics in the pre- and post-RESET regions of operation, which provide defect density information at the oxide interface with explanation of cycling issue in Al/$AlO_x$/$HfO_x$/Al structure. On the other hand, by using current-sweep operation, an early RESET event can be avoided due to reduced current induced over-heating, which provides insights and optimization for power management in $HfO_x$-based RRAM. The dynamic conductance technique and the experimental results not only help to identify resistive switching mechanisms but also construct a model to predict $HfO_x$-based RRAM device operating performance for future device designs and applications.[1]

## 2.2 DEVICE DESIGN AND FABRICATION

Al (100 nm)/$HfO_x$ (10 nm)/Al (210 nm) and Al (100 nm)/$AlO_x$ (5 nm)/ $HfO_x$ (10 nm)/Al (210 nm) bilayer-insulator devices were fabricated (see transmission electron microscope (TEM) images in Fig. 1 (a) and Fig. 1 (b)). Starting substrates are heavily-doped N+ Si wafers. First, buffered-oxide-etch (BOE) was used to remove any native oxide layer on the substrate, followed by acetone and isopropyl alcohol (IPA) rinse. Aluminum (210 nm thick) was deposited on N+ Si substrate as bottom electrode using e-beam evaporation at a pressure of less than $10^{-5}$ Torr. There may exist a thin layer (~2 nm) of unintended $AlO_x$ even though we deposited the $HfO_x$ subsequently after Al BE since Al is easily oxidized even at low temperature. This thin layer has good influence and improvement on the uniformity and reliability of performance[64]. Then, 10 nm-thick resistive switching (RS) dielectric layers of $HfO_x$ were deposited using atomic layer

[1] The content of Chapter 2 is published in "Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Fei Zhou, Meiqi Guo, Chih-Yang Lin, Cheng-Chih Hsieh, Burt Fowler, Ting-Chang Chang, and Jack C. Lee, "Dynamic Conductance Characteristics in HfOx-based Resistive Random Access Memory," RSC Advances (2017)" The author is contributed in design of experiments, sample fabrication and characterization, manuscript writing.

deposition (ALD) with precursor (TEMAH, i.e. tetrakis (ethylmethylamino)hafnium) and $H_2O$ in a ratio of 1:3 at 250 ℃. For Al (100 nm)/$AlO_x$ (5 nm)/$HfO_x$ (10 nm)/Al (210 nm) bilayer RRAM devices, the $AlO_x$ was deposited on the top of $HfO_x$ layer using ALD with precursor (TMA, i.e. trimethylaluminum) and $H_2O$ in a ratio of 2:3 at 250 ℃. $HfO_x$ was deposited using the same method described above. Then Al (100 nm) was deposited using e-beam evaporation as top electrode for both $HfO_x$ and $AlO_x$/$HfO_x$ RRAM devices. The top electrodes of various sizes (diameters of 30, 60, 150 μm) were patterned using lift-off method. Through energy dispersive spectrometer (EDS) results (data not shown), the material compositions and stoichiometry including Al top electrode, $AlO_x$ (x=1.8) and $HfO_x$ (x=2.3) of Al/$AlO_x$/$HfO_x$/Al device structure have been verified. Agilent B1500 and Lakeshore probe station were used for electrical characterization of both $HfO_x$-based RRAM structures.

### 2.3 RESULTS AND DISCUSSION

Figure 2.1 (c) and (d) show the RS I-V curves during DC voltage sweeps for $HfO_x$-based RRAM devices with and without $AlO_x$, respectively. The $AlO_x$ (5 nm)/$HfO_x$ of (3, 5 and 10 nm) stacking devices were fabricated and the performance of varied $HfO_x$ thickness has been studied. Both of switching voltage and memory window are independent of the HfOx thickness. Therefore, Al/$HfO_x$ (10 nm)/Al and Al/$AlO_x$ (5 nm)/$HfO_x$ (10 nm)/Al structures were used to demonstrate this dynamic conductance method. Voltage was applied to the top electrode (Al) with bottom electrode (Al) at ground. All the testing was done in air ambient. Unipolar switching is observed for these two device structures (Figure 2.1). First, a one-step electroforming (inset in Figure 2.1 (c)) process was used: (1) a compliance current-limited (CCL) voltage sweep to induce

soft breakdown; and (2) a forward voltage sweep to electroform the device. In other words, soft breakdown in the insulator occurs when voltage is swept until the current dramatically increases to a CCL of 1 μA. Generally, this current compliance is used to prevent hard breakdown (i.e. permanent breakdown) of oxide layers during forming process. After the electroforming, RS performance is stabilized by cycling multiple times using DC voltage sweeps. Then a SET process is applied by a forward/reverse sweep with 1 mA CCL to program the device to low resistance state (LRS). As shown in Figure 2.1 (c) and (d), the SET voltage for RRAMs with and without $AlO_x$ is approximately 2.2 V and 1.8 V, respectively. The RESET process is applied by sweeping the voltage to the value where the current decreases abruptly to program the devices to high resistance state (HRS). The RESET voltage for RRAMs with and without $AlO_x$ is approximately 1 V and 0.8 V, respectively (see Figure 2.1 (c) and (d)). The LRS/HRS current ratio is ~ $10^7$ and $10^4$ at a read voltage of 0.1 V for RRAM devices with and without $AlO_x$, respectively.

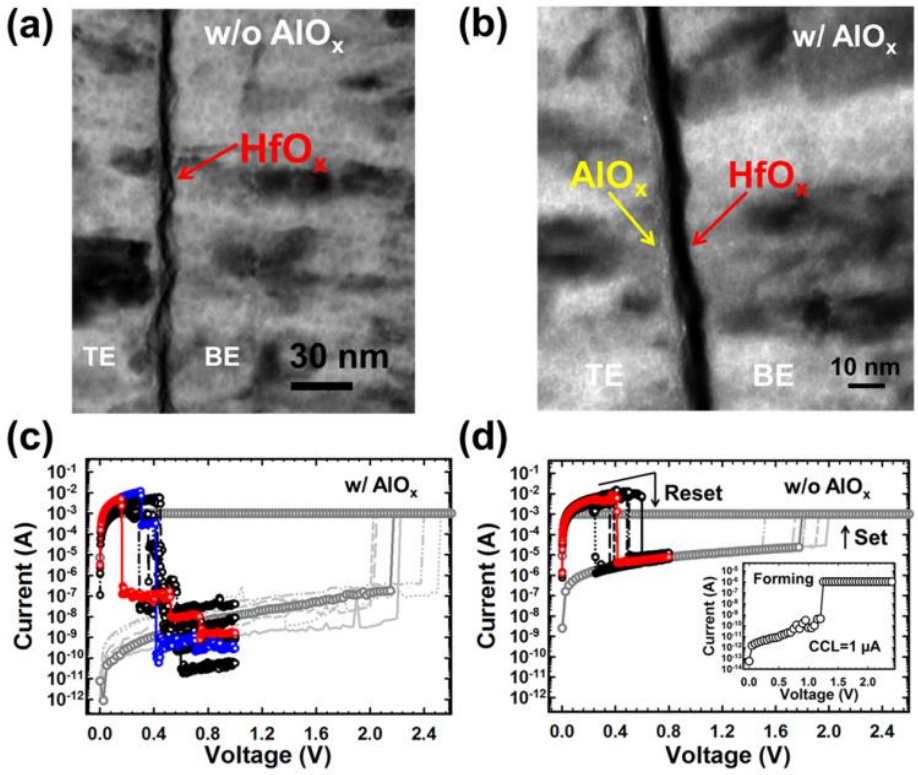



Figure. 2.1. (a) TEM cross-section image to view the interface of Al (top electrode, TE)/$HfO_x$ (10 nm)/Al (bottom electrode, BE) RRAM; (b) interface of Al (top electrode)/$AlO_x$ (5 nm)/ $HfO_x$ (10 nm)/Al (bottom electrode) RRAM; (c) I-V curve for Al/$HfO_x$(10 nm)/Al RRAM; (d) I-V curve for Al/$AlO_x$ (5nm)/$HfO_x$ (10nm)/Al RRAM.

To investigate RESET mechanisms, I-V curves were analyzed using the dynamic conductance method (i.e. $\partial I/\partial V$) in two regions (i.e., pre-RESET and post-RESET). During the RESET sweep to ~0.8-1 V, current begins to drop at RESET voltage ($V_{RESET}$) and the device is programmed to HRS. With identical SET CCL of 1 mA, multi-step-like and one-step-like RESET are observed in RRAM with and without $AlO_x$ (Figure 2.1 (c) and (d)). In other words, by adding $AlO_x$ in switching layers, the RESET I-V transition above $V_{RESET}$ changed from one-step fall-off to multiple fall-off in current resulting in

different HRS states. This difference can be contributed to the high defect density at the interface between $AlO_x$ and $HfO_x$ layers, leading to the abrupt current drop during filament rupturing in RESET process[65,66]. In contrast, the SET process shows no multiple SET behaviors in these two structures. Analyzing plots of I-V dynamic conductance (or 2nd derivative) can help understanding the RESET mechanism and further clarify the fall-off process where the filament degrades/ruptures during RESET process. Figure 2.2 (a) shows a schematic representation of the temperature dependence in the pre-RESET region, cycling capability, and device structure dependence observed in the 1st derivative/2nd derivative plots for devices with (green curve) and without $AlO_x$ (blue curve). These dynamic conductance characteristics (1st derivative/2nd derivative analyses) can help to verify that the fundamental filament degradation behaviors are enhanced in devices without $AlO_x$ compared to devices with $AlO_x$ for these variables under cycling analyses (more discussion in Figure 2.2 (c), shows that the unnecessary heat resulting in filament degradation in pre-RESET region can be avoided). For the post-RESET region, temperature dependence dynamic conductance characteristics can further confirm the statement of unnecessary heat induced filament degradation in pre-RESET region (or we called an early RESET event in LRS), and help to clarify the one-step fall-off RESET process and the multi-step fall-off current drop between these two structures (more discussion in Figure 3, diffusion-driven and electrical-driven RESET behavior). Figure 2.2 (b) shows the I-V curve and the dynamic conductance plot of RRAM devices with $AlO_x$, which provides the switching parameters, such as intercept of dynamic conductance (at 0 V), the tangential slope of the dynamic conductance at the intercept (at 0 V), and the slope of dynamic conductance (> zero bias region), as described in further detail in the Figure 2.2 (c) and Figure 2.3.

Figure 2.2 (c) shows the cycling effect on initial rate of $I_{LRS}$ increment (i.e. the first derivative) and filament degradation for the two RRAM devices. The initial rate of ILRS increment is defined as the intercept of dynamic conductance curve as shown by the red curve in Figure 2.2 (b), and filament degradation is defined as the tangential slope of the dynamic conductance at the intercept. The initial rate of $I_{LRS}$ increment is higher for RRAM devices without $AlO_x$, which indicates the RRAM without $AlO_x$ reaches the RESET current faster than RRAM with $AlO_x$ (see black curve in Figure 2.2 (c)). The initial rate of ILRS increment values in $Al/AlO_x/HfO_x/Al$ structure are quite close to zero with all 10 cycles, indicated that the filament is weaker than $Al/HfO_x/Al$ structure even at zero-bias region due to the growth of filament is limited by internal filament effect with potentially triggering the RESET event earlier (in $Al/HfO_x/Al$, the values are positive, means that the LRS or filament continues increasing or growth)[67]. A similar scenario can be observed in filament degradation analysis (blue curve in Figure 2.2 (c)), RRAM with $AlO_x$ has worse filament degradation after 8 cycles (the larger of negative values (e.g. -0.2). This implies that the filament is already in the self-compliance region (the tangential slope of the dynamic conductance has three cases; slope > 0, the filament continues growth; slope ~ 0, filament self-limiting behavior; and slope < 0, RESET transition beginning) and would run into RESET transition at the zero-bias region, which indicates that the generated current-induced Joule heating by DC cycling severely affects filament degradation rate in $Al/AlO_x/HfO_x/Al$ structure. With higher initial rate of $I_{LRS}$ increment, the unnecessary heat resulting in filament degradation in pre-RESET region can be avoided for RRAM without $AlO_x$. In other words, the RRAM without $AlO_x$ is more desirable due to potentially less electrical or thermal stress than in $Al/AlO_x/HfO_x/Al$ structure and less cycle-induced filament degradation. In addition, this filament degradation of RESET behaviors has important correlation to endurance failure.

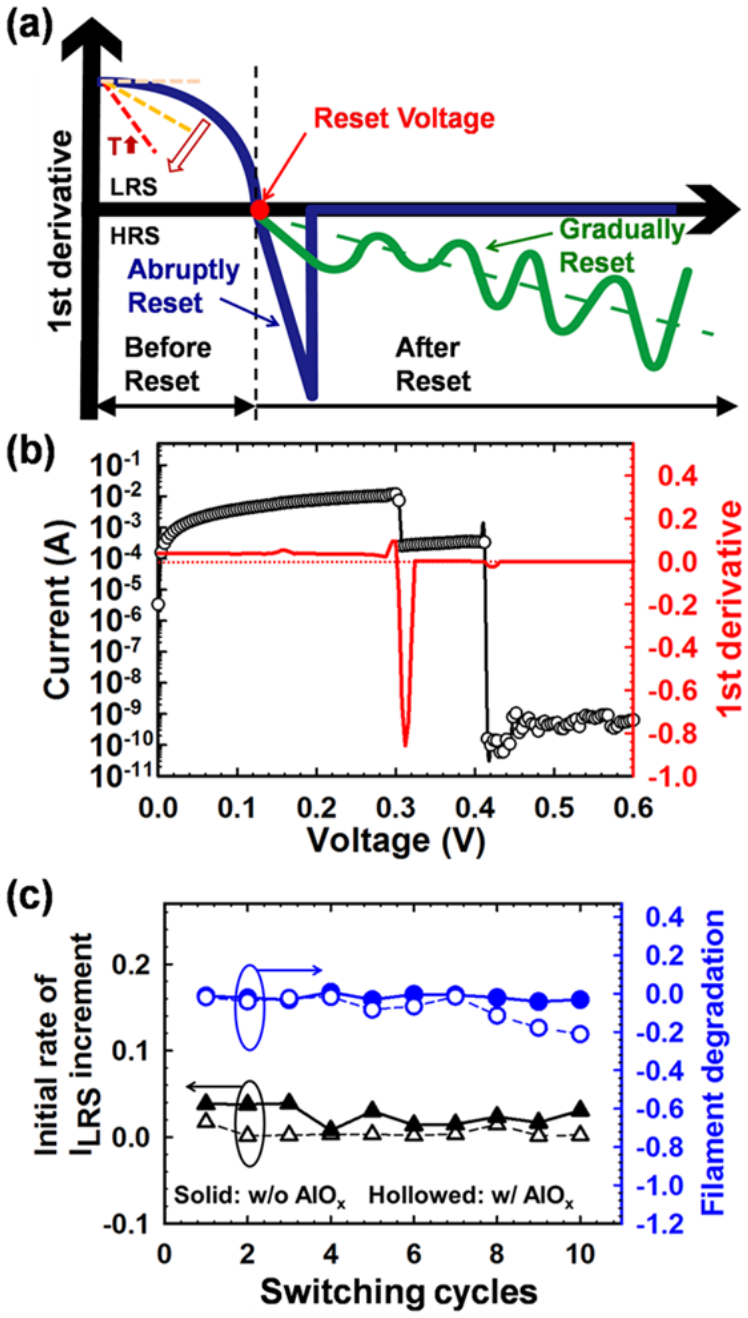



Figure 2.2. (a) Schematic of RESET analysis by dynamic conductance of I-V curve, (b) I-V curve for RESET process and dynamic conductance (w/ $AlO_x$), (c) cycling effect on initial rate of $I_{LRS}$ increment (intercept of dynamic conductance) and on filament degradation (tangent line of dynamic conductance at the intercept).

Figure 2.3 (a) shows the filament degradation as a function of operating temperature for the pre- and post-RESET regions on RRAM without $AlO_x$. The filament degradation (i.e. the slope of dynamic conductance) in the pre-RESET region (> zero bias region, as shown in Figure 2.2 (a)) is caused by a sequence of random defect events, i.e. a defect injection into the filament or extraction from the filament. The value of 2nd derivative due to dynamic resistance change of filament (Figure 2.2 (c)) is then analyzed using a linear fitting method to obtain the overall slope, which is negative in the pre-RESET region, as shown in Figure 2.2 (a). The LRS filament degradation is caused by discrete defects migration, which is correlated to a random value of activation energy (Ea) and a corresponding migration rate[65,68]. With increasing operating temperature up to 60 ºC, filament degradation begins to occur in the pre-RESET region. The filament degradation is much more severe in post-RESET (ruptured) than the pre-RESET processes at room temperature (value of -3 vs. 0). For the pre-RESET region, the filament degradation deteriorates with increasing temperature after 50 ºC (from -0.01 to -0.05). However, for the post-RESET region, the filament degradation becomes less negative with increasing temperature from 40 to 70ºC. This can be explained by diffusion-driven (i.e. highly temperature-dependent) RESET behavior in the gentle, gradual-RESET behavior other than abruptly RESET[69-71].On the other hand, the electrical-driven RESET behavior can explain the post-RESET region, i.e. the abrupt RESET with larger filament degradation (value of -3) at 20 ºC in Figure 2.3 (a).

Figure 2.3 (b) shows the non-zero fluctuation counts in 2nd derivative of the RESET I-V curve from 20 to 70 ºC. The non-zero fluctuation counts represent the observation of smooth curve-like continuous gradual RESET switching behavior instead of abrupt RESET. The more non-zero fluctuation indicates highly gradual RESET-like behavior. In pre-RESET region, the counts increase with increasing temperature due to

thermal disturbance, leading to filament degradation and increasing probability of early RESET on LRS. In other words, the increasing fluctuation may result from the increasing probability to either inject into or extract out the conductive filament even under a thicker filament condition, i.e. LRS. In the post-RESET region, the counts increase with increasing temperature up to 50 ºC showing the temperature-induced gradually RESET. This is due to the fact that the rate of defect injection exceeds the rate of extraction among the discrete defect migration during the RESET transition. This phenomenon retards after 50 ºC possibly due to current induced over-heating (or self-accelerated by Joule heating) in localized region[72], which in turn causes the abrupt RESET and highly efficient rupture of filament. Thus, by suppressing the accelerated self-heating process in unipolar-type resistive switching, a precise control of filaments temperature and localized switching phenomena can be achieved. This provides possible solution for early RESET event on LRS[73, 74].

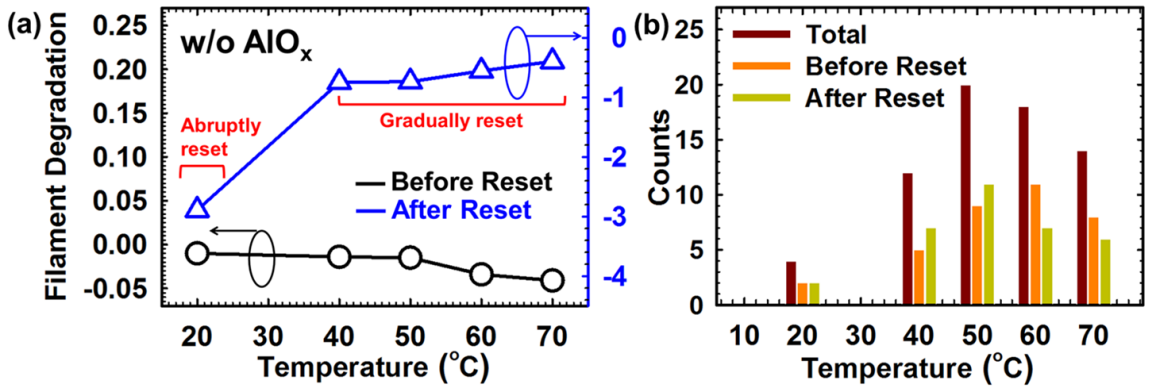



Figure 2.3. (a) Filament degradation as a function of temperature pre- and post- RESET, (b) non-zero counts in 2nd derivative.

Figure 2.4 and Figure 2.5 show the data obtained by current-sweep technique during the SET process. The current sweep technique is known to prevent device hard-

breakdown and current overshoot failures (i.e. less electrical and thermal stress)[75]. The typical current-sweep I-V curves of Al/$HfO_x$/Al and TaN/$HfO_x$/Al devices are shown in Figure 2.4. In contrast to the I-V curves using voltage-sweep, there are multiple states observed between the LRS and HRS in both Al/$HfO_x$/Al and TaN/$HfO_x$/Al RRAM devices. These multiple intermediate states can potentially be used for multi-level memory application by controlling the CCL in SET process and RESET stop voltage in RESET process, respectively. Meanwhile, the snap-back voltage, i.e. the maximum sensing voltage, can be observed during the current-sweep process, where the resistance state begins to change from HRS to LRS. Through the SET process, the voltage across the device continues to increase as the current is swept up until the certain current endpoint is reached, i.e. LRS, where is the "snap back voltage." The multiple voltage snap-back observation reflects the gradual RESET process of the conductive filament, suggesting that the broken conductive filament builds up again gradually in $HfO_x$ layer[76].The SET voltage is relatively higher in Al/$HfO_x$/Al than in TaN/$HfO_x$/Al devices potentially due the competitive oxygen vacancies affinity between Al electrode and TaN electrode, e.g. the enthalpy of formation for of TaN and Al, -252.3 kJ/mol and 577.5 kJ/mol, respectively[77-78].

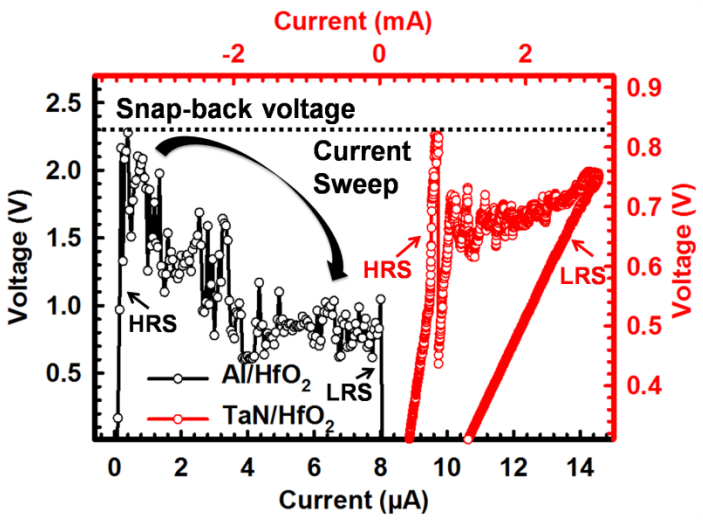



Figure 2.4. Typical I-V relation of in Al/$HfO_x$ (5 nm) (black) and TaN/$HfO_x$ (5 nm) (red) in SET process by using I-sweep. The black arrow indicates the current sweeping directions. The holding voltage is defined as the "end" of sensing voltage immediately before the memory state abruptly drops from HRS to LRS, i.e. at the end of the snap-back process by I-sweep.

The effect of device area by current-sweep in Al/$HfO_x$/Al device compared to voltage-sweep measurement technique is shown in Figure 2.5 (a) and Figure 2.5 (b). It has been found that LRS and HRS current (Figure 2.5 (a)), as well as the SET and RESET voltages (Figure 2.5 (b)), are independent of device area, illustrating that charge transport and RS occurs in a localized region along a conductive filament[79]. Consistently, it provides further switching voltage reduction by using current-sweep (Figure 2.5 (b), 0.6 V - 1.4 V for current-sweep and 1.5 V – 2.8 V for voltage-sweep). This voltage reduction may be resulted from heat-induced defect injection that could improve the programming efficiency than an electrical-field driven process in a localized region along a conductive filament. The structure of filament changes due to defect injection/extraction during programing[80]. The current sweep technique not only improves data acquisition and enhances the understanding of the physics related to the SET

process, but also provides the power management capability in localized region for further reduction of current induced over-heating in an early RESET event on LRS.

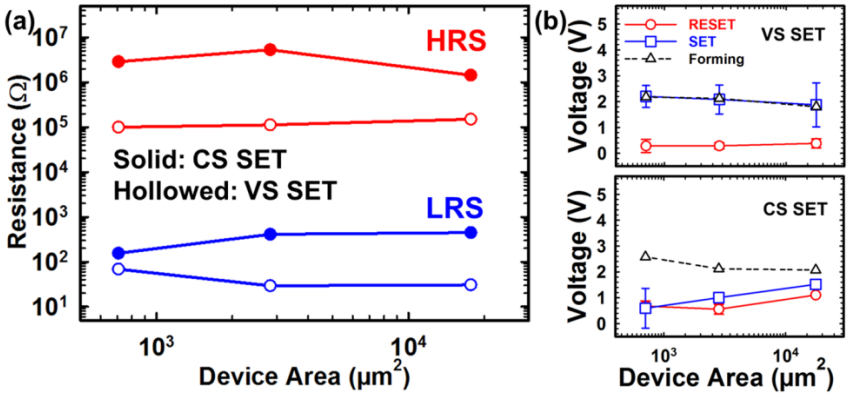



Figure 2.5. Device area effect of Al/HfOx/Al RRAM (a) on the HRS and LRS, (b) on forming and switching voltage by voltage-sweep (VS) and current-sweep (CS).

## 2.4 CONCLUSION

In conclusion, early partial RESET phenomenon has been investigated using dynamic conductance analysis, and the SET voltage has been found to reduce using a current-sweep programing method in comparison to voltage-sweep method. High on/off current ratios of ~$10^4$ with suitable switching voltage (< 2 V) for Al/$HfO_x$/Al RRAM have been obtained. Through dynamic conductance analysis, one-step-like and multi-step-like RESET behaviors in the pre-RESET and post-RESET regions have been investigated. Partial RESET within the pre-RESET region has been observed in Al/$AlO_x$/$HfO_x$/Al RRAM by cycling test, owing to high defect density at the $AlO_x$/$HfO_x$ interface. The filament degradation phenomenon in the pre-RESET region deteriorates with increasing temperature. By using current-sweep technique, the SET voltage has been reduced to half of that obtained by voltage-sweep operation, which provides advantages

of less electrical and thermal stress for power management capability in localized region for future low power applications.

# Chapter 3: Bilayer Oxide-based Selectorless RRAM with Internal Gap Design by Compliance Current Limit (CCL) Modulation

## 3.1 INTRODUCTION

Among the emerging memory technology, resistive random-access memory (RRAM) device holds great potential as an emerging candidate because of its simple design, high-speed operation, excellent scalability and low power consumption. However, the sneak path current ($I_{sneak}$) through unselected neighboring cells is a major problem in crossbar RRAM array configuration, which significantly affects the read operation and accuracy. To address the sneak path current issue, a transistor or a selector device is typically integrated with the memory device. Unfortunately, integrating an additional selector device, i.e. 1T-1R and 1S-1R configurations, considerably increase the manufacturing complexity and cost while limiting the scalability. In order to reduce the process complexity and cost for future microelectronic scaling, the selectorless 1R-only RRAM is proposed for suppressing the sneak path current without utilizing a selector device (Figure 3.1). Bilayer selectorlessRRAMs have been demonstrated by utilizing the intrinsic nonlinear resistive switching (RS) characteristics, without an additional transistor or a selector, which lowers the process complexity and cost. The bilayer structures i.e. high-k layer/low-k layer stacks are beneficial in superior scalability, while suppressing the sneak path currents and reduce the error in crossbar RRAM array. The sneak-path leakage current issue is the severe hindrances for the application of high-density memory crossbar array design. This chapter, experimentally presents the nonlinearity intended physical design in $HfO_x$-based RRAM devices through controlling

of SET compliance current limit (CCL) electrically with a low effective dielectric constant inserted layer (i.e. $SiO_x$) for bipolar low-voltage operating selector-less memory devices. This demonstrates the intrinsic nonlinear resistive switching characteristics of $HfO_x/SiO_x$-based stacking structure as a realization for selectorless RRAM devices. The NL characteristic was obtained and designed by optimizing the internal filament location with low effective dielectric constant layer intending in $HfO_x/SiO_x$ structure. The stacking $HfO_x/SiO_x$-based RRAM device as the one-resistor-only memory cell is applicable without additional selector device to solve the sneak-path issue with switching voltage ~1 V, which is desirable for low power operating in built-in nonlinearity crossbar array configuration. This chapter not only proposes a possible NL improvement method through an additional device-level design freedom in NL, but also provides a potential progress for high-density RRAM array commercialization.[2]

[2] The content of Chapter 3 is published in:
Ying-Chen Chen, Chih-Yang Lin, Hui-Chun Huang, Sungjun Kim, Burt Fowler, Yao-Feng Chang, Xiaohan Wu, Gaobo Xu, Ting-Chang Chang, and Jack C. Lee. "Internal Filament Modulation in Low-dielectric Gap Design for Built-in Selector-less Resistive Switching Memory Application." Journal of Physics D: Applied Physics (2018),"
Ying-Chen Chen, Chao-Cheng Lin, Sungjun Kim, and Jack C. Lee, "Selectorless Oxide-based Resistive Switching Memory with Nonuniform Dielectric for Low Power Crossbar Array Applications" ECS Transactions (2019),
Ying-Chen Chen, Hui-Chun Huang, Chih-Yang Lin, Sungjun Kim, Yao-Feng Chang, and Jack C. Lee "Effects of ambient sensing on SiOx-based resistive switching and resilience modulation by stacking engineering" ECS Journal of Solid State Science and Technology (2018),
The content of Chapter 2 is published in "Ying-Chen Chen, Yao-Feng Chang, Xiaohan Wu, Fei Zhou, Meiqi Guo, Chih-Yang Lin, Cheng-Chih Hsieh, Burt Fowler, Ting-Chang Chang, and Jack C. Lee, "Dynamic Conductance Characteristics in HfOx-based Resistive Random Access Memory," RSC Advances (2017)
The author is contributed in design of experiments, characterizations, manuscript writing.

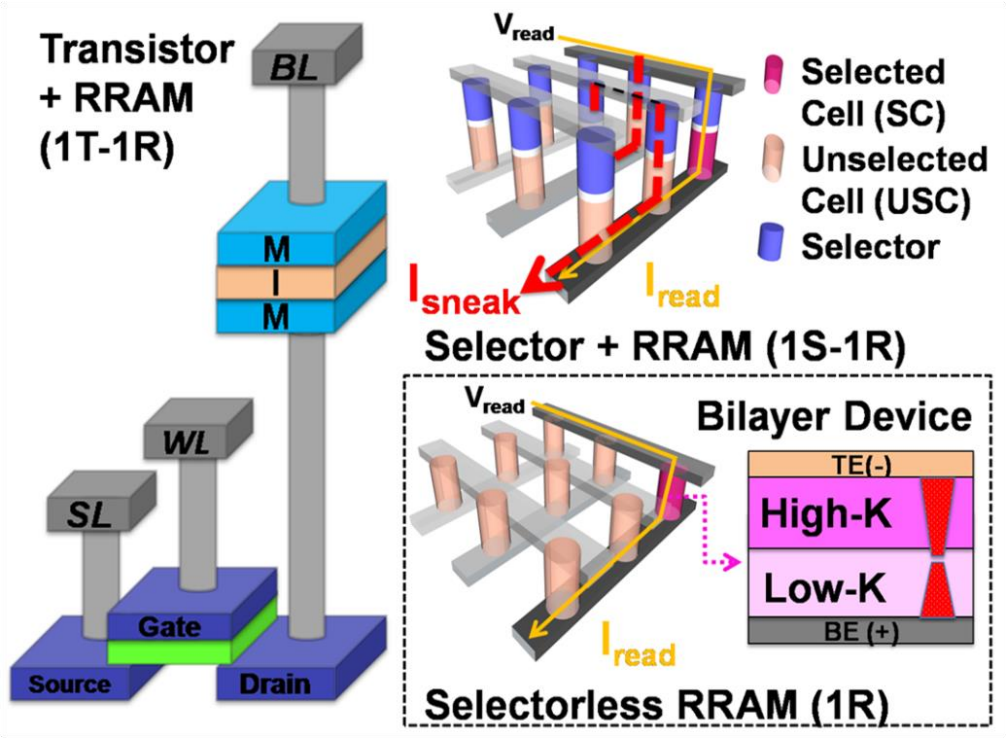



Figure 3.1. Schematics of regular 1 transistor +1 memory (1T-1R), 1 selector +1 memory (1S-1R) configuration, and proposed 1R-only selectorless RRAM with bilayer design by effective dielectric constant modulation for selectorless RRAMs.

## 3.2 Device Design and Fabrication

### 3.2.1 $HfO_x$, $SiO_x$ single layer RRAM and $HfO_x/SiO_x$ Stacked RRAM

Selector-less RRAM devices with varying length of side in square of 400 nm, 600 nm, 800 nm, 1 $\mu$m, 4 $\mu$m have been fabricated. The starting substrates are heavily-doped N+ Si wafers. First, buffered-oxide-etch (BOE) was used to remove any native oxide layer on the substrate, followed by acetone and isopropyl alcohol (IPA) rinses. Titanium nitride of 200 nm thickness was deposited on $N^+$ Si substrate as bottom electrode using an RF sputtering system at a pressure of less than $10^{-5}$ torr. Then, 9 nm of

$SiO_x$ and 4 nm of $HfO_x$ were deposited as RS dielectric layers for bilayer structures by RF sputtering continuously without breaking the vacuum.

Then, Pt (165 nm) was deposited as top electrodes for bilayer ($HfO_x/SiO_x$) RRAM devices. Meanwhile, RRAM structures with single $HfO_x$ layer and single $SiO_x$ layer have been fabricated as references. Conventional photolithography was used for patterning the top electrodes of various sizes using the lift-off method. Finally, Pt (165 nm)/$HfO_x$ (4 nm)/$SiO_x$ (9 nm)/ TiN (200 nm) and Pt (165 nm)/$HfO_x$ (4 nm)/$SiO_x$ (9 nm)/ $HfO_x$ (4nm)/ TiN (200 nm) devices were fabricated as bilayer and trilayer devices. An Agilent B1500 and Lakeshore probe station was used for electrical characterization of all the $SiO_x$-based stacking RRAM devices.

## 3.3 CHARACTERIZATION

### 3.3.1 Nonlinear I-V curve and electrical characteristics

The intrinsic nonlinear nature in a selectorless RRAM can alleviate the sneak path current because the on-state of the selected cell (SC) is read at a "high-voltage" region, while the sharp conductance decrease at "low-voltage region" effectively suppresses the sneak current through the unselected cells (USC) (Figure 3.2). For single layer $SiO_2$ RRAM devices, the carrier transport behaviors have been widely studied[81-84]. The results show that LRS current transport mechanism in single layer $SiO_2$ RRAM devices are driven by exponential-type (P-F emission, Hopping process, or trap assisted tunneling model) current behaviors, which means that for single layer $SiO_2$ RRAM devices, the non-linearity type I-V characteristics in LRS has better NL as compared to single layer

$HfO_2$ RRAM device. In most cases, the LRS in $HfO_2$ RRAM device has been studied as Ohmic behavior or shallow defect energy level / lower energy barrier height in non-linearity type I-V characteristics as well, based on the CCL control[62]. From a physics viewpoint, a single layer $SiO_2$ RRAM device shows a larger effective trap depth below the conduction band as compared to single layer $HfO_2$ RRAM device, which means that the non-linearity level would be much more obvious in single layer $SiO_2$ RRAM devices than single layer $HfO_2$ RRAM devices. Therefore, $SiO_2$ show better NL than $HfO_2$. Of note, for bilayer layer RRAM device, even the effective trap depth below conduction band is shallower than single layer $HfO_2$ RRAM devices, however, due to the switching gap in low-k region, the NL is still better than single layer $HfO_2$ RRAM devices. In a physic viewpoint, the $SiO_x$ layer can be used as a layer to reduce the HRS and LRS current due to lower dielectric constant, which has less oxygen vacancies concentration than $HfO_x$ layer. In this way, the $SiO_x$ is viewed as a candidate for the low-k material in stacks for selectorless RRAM devices. According to current reports for metal oxide memristors, the electroforming and switching voltages of $SiO_x$ are known as higher than $HfO_x$ due to lower oxygen vacancy/defects concentrations[81-83].

Figure 3.2 (a) shows bipolar RS I-V characteristics during DC voltage sweeps for the single $HfO_x$ layer and bilayer stacking RRAM devices. Voltage was applied to the bottom electrode (TiN) with the top electrode (Pt) at the ground. All the electrical testing was done in air environment instead of under vacuum as in previous works[81-83]. To initiate the RS in these devices, a one-step single sweep electroforming (data not shown) process was used: (1) a current-limited voltage sweep to induce soft breakdown; and (2) a

forward voltage sweep to electroform the device. In this work, the soft-breakdown process is performed by sweeping the voltage until current dramatically increases to a CCL of 1 mA. Generally, this current compliance is required to prevent permanent hard-breakdown of oxide layers during the forming process and increases the "electroforming yield" for RRAM devices, i.e. % of good devices after electroforming. After the electroformation, RS performance is stabilized by cycling multiple times (e.g. 30 cycles in this work) using DC voltage sweeps. The SET process i.e. switching from HRS to LRS takes place in positive polarity while the RESET occurs in negative polarity. The in I-V characteristics of five structures are compared in terms of RS voltage, current, and NL behaviors. The SET voltage of the five structures is ~1 V forward/reverse sweep with 1 mA CCL to program the device to LRS. The RESET process is done by sweeping voltage to -2.1 V for all RRAM structures, where current decreases as the voltage is swept from around RESET voltage (e.g. -1 V for bilayer structure) and the devices are programmed into a HRS. Comparing the bilayer structure as $HfO_x$ (4 nm)/$SiO_x$(9 nm) (H4S9, red curve) to the single-layer structure with $HfO_x$ of 11 nm (H11, dark curve), the LRS current at -0.2 V is reduced from ~$10^{-3}$ to ~$10^{-5}$ A. It could be seen that there was significantly increased resistance at the low voltage region. This NL characteristic observed in RRAM can be used to solve the problem of interference from neighbor cells in a cross-bar array. Since the current dropped in the low voltage region in the bilayer structure unlike in the single $HfO_x$ layer device, the NL characteristics can be utilized for avoiding sneak path issue and read error in array applications. Instead of fabricating 1S1R by relatively complicated processes and larger feature size, this bilayer stacking

structure can realize highly scalability with nonlinearity, so-called selector-less RRAM devices. It depicts that using $SiO_x$ as a stacking layer improves the nonlinearity characteristics. The presence of a $TiO_x$ layer between TiN and $SiO_x$ layer are exists due to the non-break out PVD process during layer deposition. However, by changing the thickness of the $SiO_x$ and $HfO_x$ layer, the NL is different (discussed in chapter 4), which is independent of $TiO_x$ existing in the stacking process. Therefore, the presence of a $TiO_x$ layer effect is avoided in the device analysis ($TiO_x$ dielectric constant is around 80, which is higher than $HfO_x$ layer as well as $SiO_x$ layer[85]).

In order to understand the NL characteristics in $I_{LRS}$ by utilizing the bilayer structures, the device-to-device (D2D) and cycle-to-cycle (C2C) variation have been investigated in Figure 3.2. (b) (read at -0.6V). There are fifteen tested devices for each structure, and 30 DC cycles are tested for each device. The considerable improvement of nonlinearity in $HfO_x$ (4 nm)/$SiO_x$ (9 nm) of ~28 (D2D) and ~22 (C2C) at CCL of 1 mA has been observed systematically with these statistic results, as a comparison of $HfO_x$ single layer. Based on the results, inserting a low-k material layer can be thought of as a plausible way to suppress the sneak path current in crossbar RRAM array. The statistic results of the LRS variability with cycling tests have also been studied, which is below 1 order and is not likely to affect the function of NL in selectorless RRAM (data not show here). Furthermore, nonlinearity is the major parameter that affects the sneak path currents. In this way, the nonlinearity characteristics of bilayer devices can be utilized to suppress the sneak path currents. With a thin $SiO_x$ layer (2 nm) on the bottom of $HfO_x$ (11 nm) layer i.e. H11S2, the NL has become doubled to single $HfO_x$ layer device and

enlargedthe array size. Based on these results, the bilayer RRAM device was found to show the highest NL among the $SiO_x$-based stacking structures due to a low effective dielectric constant inserted layer. The NL of the bilayer structure is better than single layered $HfO_x$ devices, which makes $SiO_x$-based bilayer devices as a potential candidate for selector-less RRAMs. The NL characteristics as a function of SET CCL for bilayer, trilayer and single layer devices are shown in Figure 3.2 (c). The NL is the average result of 30 cycles for each data point. According to the results, the NL characteristics are improved by using $SiO_x$-based stacking structures instead of the $HfO_x$ single layer (NL <5). Of note, for $HfO_x$ single layered device, the existing NL (not Ohmic behavior) and semiconductor-type temperature-dependence carrier transport response shows that the remained GAP existing as considered discontinuous conductive filament (discussed later in Figure 3.4). In addition, NL has an optimized value with controlling SET CCL in all the $SiO_x$-based structures, but not in $HfO_x$ single layer structure. For example, NL is ~5x of which with 1 mA SET CCL than of which with 0.3 mA in bilayer structure. With small SET CCL i.e. 0.3 and 0.5 mA in a bilayer structure, the $I_{LRS}$ at $V_{read}$ is restricted near the CCL at low voltage region and lower the NL value, meanwhile, there is a significant resistance drop in terms of the higher CCL (i.e. 2 and 3 mA) which deteriorate the NL characteristics. The expected scalability of the stack i.e. total thickness can be further reduced to below 10 nm if implemented the 1R-only process integration with better CCL control.

Figure 3.2 (d) shows device structure effects on SET switching voltages (upper panel) and RESET switching currents (bottom panel), where dependencies are observed

primarily for SET voltage. The benefit of $HfO_x$-based devices (single/double/tri-layer) is the lower switching voltages, whereas the single layer $SiO_x$-based device hashigher switching voltage values. $HfO_x$ may act as an effective oxygen getter to help remove liberated $O_2$ ions from the filament as it is being formed. Figure 3.2 (d) bottom panel shows the RESETcurrent is independent of a device structure.

Figure 3.2 (e) shows the data retention result depicts that LRS/HRS are stable for bilayer with the resistance ratio of 2 orders of magnitude, and no significant degradation is observed for more than $10^4$ s, further confirming the excellent nonvolatile properties of the $SiO_x$-based RRAM devices. In spite of the larger resistance ratio ~4 orders of magnitude observed in trilayer structures, the retention behavior degraded after ~100 sec. The degradation of trilayer device is ~1812 %, which is severe in LRS rather than HRS. This is suggested that trilayer structure has one more material interface i.e. $HfO_x$ and $SiO_x$ interface than bilayer, and the higher oxygen vacancy concentration resulting in the unstabilized oxygen exchange layer and early retention degradation[65, 88]. Figure 3.2(f) shows HRS and LRS resistance for >1000 AC pulse switching cycles for an endurance test. A resistance ratio can clearly shrink to less than 1 order of magnitude after cycling (driven by HRS degradation mostly), which may be driven by accumulated vacancies generation in overshoot effect[89-90].

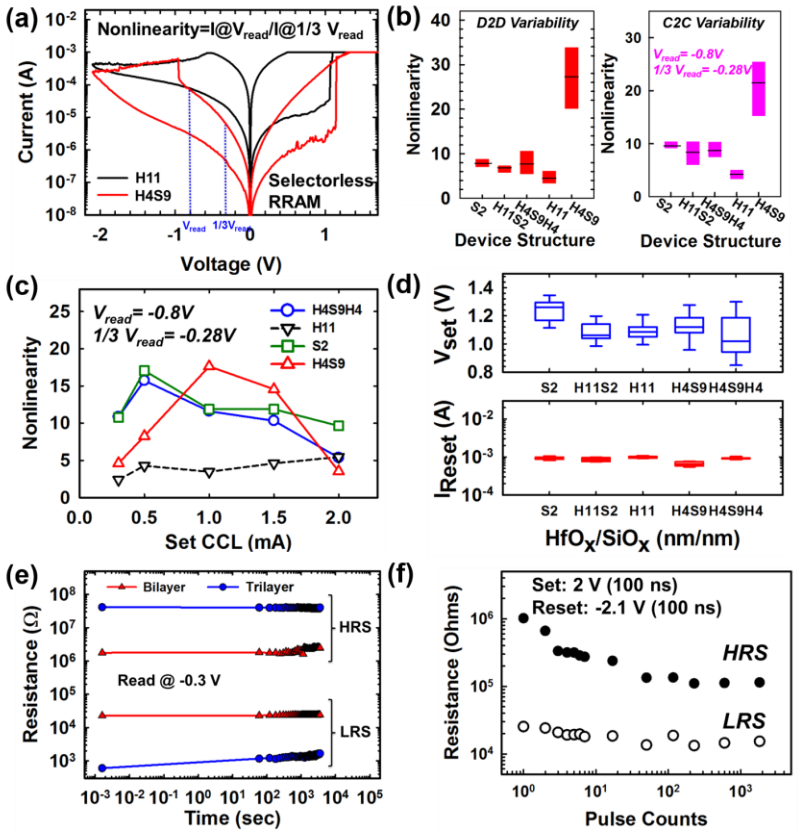



Figure. 3.2. (a) Bipolar I-V characteristics for SET and RESET resistive switching of linear RRAM and nonlinear selector-less RRAM. (b) Nonlinearity characteristics and device-to-device, cycle-to-cycle variability for five structures. (c) Nonlinearity as a function of SET CCL in bilayer (H4S9 and H11S2), trilayer (H4S9H4), single layer HfOx (H11), single layer SiOx (S2) structures with read voltage of -0.8 V. (d) SET voltage (upper panel) and RESET current (bottom panel) for five structures.(e) Retention measurement results of bilayer and trilayer structures. (f) HRS and LRS endurance data of bilayer structure during AC voltage cycling.

### 3.3.2 Current transport mechanism

The SET process programs the device to a conductive, low-resistance state (LRS). The RESET process programs each device to a low-conductance, high-resistance state (HRS). The TEM image of H4S9 is as showed in Figure 3.3 (a). First, the basic current transport mechanism in devices need to be investigated, and Figure 3.3 (b) shows the I-V

data were analyzed by normalized conductance method with fitting to common insulator charge transport expressions.

Table 3.1. Voltage dependence of current (I) and normalized conductance (GN), and the axes used for linear fitting are listed for common insulator charge transport expressions.

| Transport | $I$ | $G_N$ | Linear Fitting |
|---|---|---|---|
| Poole-Frenkel | $gVe^{\beta\sqrt{V}}$ | $1+\beta\sqrt{V}/2$ | $\ln(I/V)$ vs$V^{1/2}$ |
| Fowler-Nordheim | $AV^2e^{-B/V}$ | $2 + B/V$ | $\ln(I/V^2)$ vs $1/V$ |
| Schottky | $I_oe^{\rho\sqrt{V}}$ | $\rho\sqrt{V}/2$ | $\ln(I)$ vs$V^{1/2}$ |
| Power Law | $MV^p$ | $p$ | $\ln(I)$ vs$\ln(V)$ |

Table 3.1 lists the voltage dependence of current and normalized conductance ($G_N$) for the four insulator charge transport expressions, the voltage dependence of current and normalized conductance $G_N$ has been used as the analysis method,[81-87,62] where $G_N=G/G_0$, with dynamic conductance being given by $\partial I/\partial V$ (1st derivative) and static conductance being $G_0 = I/V$. The graphs of $G_N$ can help identify the active charge transport mechanism and the voltages where the charge mechanism change happens. For NL region of LRS, as shown in Figure. 3.3 (b), the I-V data of bilayer structure has been analyzed in a low voltage region. The $G_N$ plots in both temperature and CCL effects have an intercept near unity (~1). Therefore, the Schottky thermal emission (where the intercept would be close to 0), space charge limited current according to Child's Law (where I is proportional to $V^2$ so the intercept would be 2) are ruled out. Based on the above discussions, the Poole-Frenkel (P-F) emission is considered as the possible charge transport mechanism for current in low voltage region from 0 to -0.17 V. Similar examination procedure also

applied to various kinds of device structures (data not shown here). To further demonstrate and understand the NL intended physical design in $HfO_x$-based RRAM devices, Figure 3.3(c) shows a schematic of a prediction for resistive switching localized gap in three different devices, such as $HfO_x$ single layer, $SiO_x$ single layer, and bilayer structures, and formula derivate procedure in NL relationship by Poole-Frenkel emission transport. In the recent research, the switching model in $SiO_x$-based RRAM device assumes that the GAP region is the only part of the filament that changes resistance, and that the GAP resistance, is modulated by defect transformations between the oxygen vacancies and ions; for $HfO_x$-based RRAM system, the switching model assumes that the GAP region consider as discontinuous conductive filament constructed with the elemental Hf, and the GAP resistance is modulated by oxide chemical bond redox reactions. Both material systems show nonlinear I-V response for carrier transport behaviors in the portion of the conductive filament on either side of the GAP (conceptual "filament/GAP" model)[91-92, 62].The controlling of SET compliance current limit (CCL) electrically (fully discussed in Figure 3.5) as shown in Figure 3.2 (c), bilayer structure with a low effective dielectric constant inserted layer ($SiO_x$) (as shown in Figure 3.3 (d), formula (5)) help for low power operating selectorless memory devices. Based on Fig.3 (d) formula derivation, the nonlinearity is inverse promotional to dielectric layer properties by the carrier transport behaviors, which means that the nonlinearity is higher for lower relative dielectric constant in the GAP region. For the bilayer structure, if the filament located in the high-k region, based on the P-F formula derived, the NL has no change as compared to the single layer$HfO_x$-based device, which is a consistent with the

experimental observation. Furthermore, NL is quite close to single layer $SiO_x$-based device during CCL optimization, which is consist with the formula derivation.

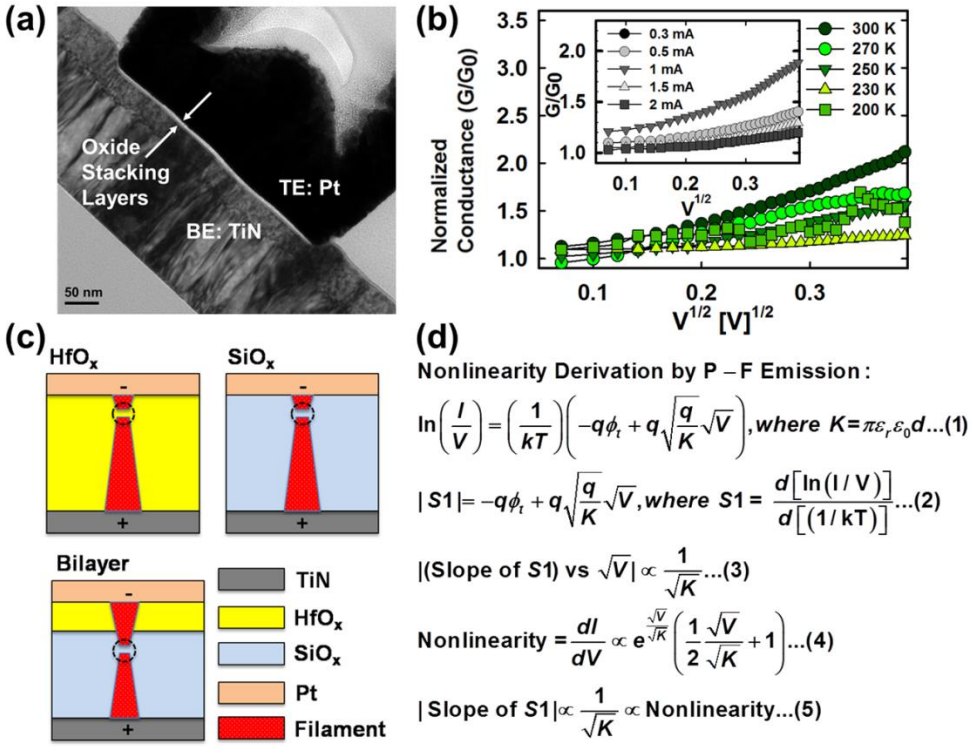



Figure 3.3. (a) TEM cross-section image to view the interface of Pt (top electrode, TE)/HfOx (4 nm)/SiOx (9 nm)/TiN (bottom electrode, BE) RRAM. (b) The normalized conductance of LRS in bilayer structure as a function of temperature and SET CCL (inset). (c) Schematics of RS regions in HfOx single layer, SiOx single layer, and bilayer structures. (d) Summary of internal filament gap design by Poole-Frenkel formula in (1) DC response, where B is a constant, q is the elementary charge, φt is the energy barrier that must be overcome by the electron, εr is relative permittivity of the RS medium, d is gap thickness, k is the Boltzmann constant and T is temperature. (2)-(3) derivate procedure from Poole-Frenkel formula. (4) Nonlinearity definition and derivate procedure. (5) The relationship between Poole-Frenkel carrier transport and nonlinearity.

### 3.3.3. Gap design method: SET compliance current limit (CCL)

Figure 3.4 (a) shows the parameters extraction in three different devices, such as $HfO_x$ single layer, $SiO_x$ single layer, and bilayer structures by temperature-dependence

Poole-Frenkel emission transport. The left panel in Figure 3.4 (a) shows the temperature-dependence of P-F fitting results for LRS with SET CCL from 0.3 mA to 2 mA in $HfO_x$ single layer structure (semiconductor-type current transport behaviors, current increasing with temperature increasing) and right panel indicates that energy barrier is ~ 0.3 eV for $SiO_x$ structure and ~ 0.12 eV for $HfO_x$ and ~ 0.06 eV for bilayer structure as V approaches 0. According to Poole-Frenkel current transport equation, the effective dielectric constant (K) is defined as $\pi\varepsilon_0\varepsilon_r d$, $\varepsilon_0$ is the permittivity in vacuum, $\varepsilon_r$ is the effective permittivity and d is the height of localized filament gap region. By equation derivation (Figure 3.3(d), from equation (1) to equation (3)), where the S1 is the slope of the plot, ln(I/V) versus (1/kT) as shown in the left panel of Figure 3.4 (a). Note that the equivalent K of each curve can be extracted from Figure 3.4 (a).However, due to the unknown localizationtemperature difference within a device, the k-values would be quite higher than expected due to the un-calibration issue of localization temperature effect.[32] The slope of S1 in the plot of energy barrier height versus $V^{0.5}$ is reversely proportional to square root of K (Figure 3.3 (d), equation (3)). On the other hand, nonlinearity defined as dI/dV of LRS is also reversely proportional to square root of K by the derivation of Poole-Frenkel emission equation (Figure 3.3 (d), equation (4)-(5)). In other words, by modulating the internal filament gap region to a material with lower effective dielectric constant K is desired to obtain good NL characteristics by stacking engineering as proposed (Figure 3.3 (d), equation (5)).

After electroforming, the geometry of filament and RS gap were stabilized by the 30 RS cycling sweeps in each structure at chosen SET CCL. Figure 4 (b) shows the SET

CCL effect on nonlinearity and K has been studied in bilayer structure. First, the square root of K is reversely proportional to nonlinearity, as discussed above and is well corresponding to equation (5). Second, nonlinearity has an optimized value with certain SET CCL in different structures (e.g. 1 mA for bilayer structure), as mentioned in Figure 3.2 (c). Here, as suggested the RS gap location is related to filament geometry i.e. diameter, which is determined by choosing SET CCL. For bilayer structure, if the gap located in low-K material e.g. $SiO_x$, the optimized nonlinearity can be obtained. Otherwise, RS gap locating in the high relative dielectric constant material with higher defect density for recombination deteriorates the LRS nonlinear behavior. The relation of nonlinearity behaviors and calculated K is shown in Figure 3.4. (c). The results seem to suggest that switching in $SiO_x$ layer (low dielectric constant) would provide increased nonlinearity than switching occurring in $HfO_x$ layer (high dielectric constant). The SET and RESET switching power are ~$10^3$ W for each of the 5 structures, which is calculated by resistive switching voltage times current. Further investigation through TEM for microstructure and physical observation of switching are in progress. The NL behavior differences of LRS in I-V characteristics between $SiO_x$-based structures (i.e. $SiO_x$ single layer and bilayer structures) and $HfO_x$-based structures are suggested to be attributed to inherent different defect-driven mechanisms resulting in varied RS gap location,[81, 95-97] which changes the heights of localized filament gap (d) in the dielectric constant values. Figure 3.4(d) shows the array size extraction by 10% read margincriteria for device structure and CCL effect. The read margin was calculated using the V/3 scheme in a cross-point array[96]. As the selected bit number increases, the energy consumption

increases more significantly by utilizing the V/2 read scheme than by V/3 read scheme. Also, as the array size is larger than 64x64, the energy consumption of ½ read scheme exceeds the 1/3 read. As a result, 1/3 read is used as the read scheme in this work. The array size is larger in $HfO_x$ (4 nm)/$SiO_x$ (9 nm) stacked devices than single-layered devices. Although we have demonstrated a possible NL modulation method was demonstrated based on the gap design by layer stacking engineer and electrical manipulation, further improvement the NL for large-scale RRAM array design is needed and in progress. The array size of bilayer device is larger than that of the single layered device with the optimized CCL. Even though NL of the bilayer device (CCL = 1 mA), may not be excellent enough to realize ultra high-density memory, the nonlinearity can be further boosted when merging with preferred low-k materials.

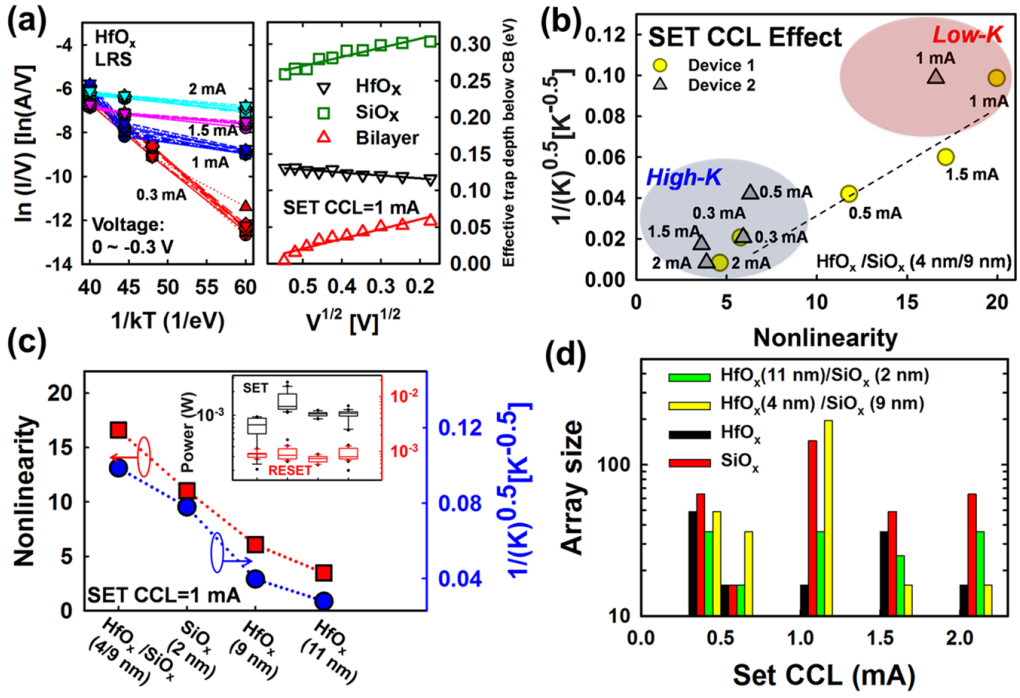



Figure 3.4. (a) Poole-Frenkel emission analysis results in low voltage region (0 V- (-0.3 V)) showing plots of ln (I/V) versus 1/kT (left panel) and calculated energy barrier versus V1/2 (right panel) of LRS for $HfO_x$ single layer, $SiO_x$ single layer and bilayer structures. (b) Calculated effective dielectric constant (K) as a function of nonlinearity in a bilayer structure, (c) Nonlinearity and 1/square root of effective dielectric constant (K) in the bilayer, single layer $SiO_x$, single layer $HfO_x$ structures (SET CCL= 1 mA) with SET/RESET power of ~$10^{-3}$ W (inset). (d) Array size extraction by 10% read margin criteria for device structure and CCL effect (0.3, 0.5, 1, 1.5, 2 mA).

The NL of the bilayer structure is better than single layered $HfO_x$ devices, which makes $SiO_x$-based bilayer devices as a potential candidate for selectorless RRAMs. The NL characteristics as a function of SET CCL for bilayer, trilayer and single layer devices are shown in Figure 3.2. (c). The NL is the average result of 30 cycles for each data point. According to the results, the NL characteristics are improved by using $SiO_x$-based stacking structures instead of the $HfO_x$ single layer (NL <5). Of note, for $HfO_x$ single

layered device, the existing NLand semiconductor-type temperature-dependence carrier transport response (Figure 3.4 (a), left panel) shows that the remained GAP existing as considered discontinuous conductive filament. In addition, NL has an optimized value with controlling SET CCL in all the $SiO_x$-based structures, but not in $HfO_x$ single layer structure. For example, NL is ~5x of which with 1 mA SET CCL than of which with 0.3 mA in bilayer structure. With small SET CCL i.e. 0.3 and 0.5 mA in a bilayer structure, the $I_{LRS}$ at $V_{read}$ is restricted near the CCL at low voltage region and lower the NL value, meanwhile, there is a significant resistance drop with the higher CCL (i.e. 2 and 3 mA) which deteriorate the NL characteristics.

In order to understand and further control the existing NL behavior in stacked RRAM structures, the gap modulation method is proposed as a possible mechanism in Figure 3.5. The NL has been measured in low SET CCL range and high SET CCL range to confirm that there is a filament diameter enlargement with increasing SET CCL (0.01 mA to 1 mA) and leads to the switching gap migration from the $HfO_x$ (high-k layer) to $SiO_x$ layer (low-k layer). If the filament switching gap is fixed in $HfO_x$ layer, the NL has no differences with increasing SET CCL (see Figure 3.2 (c) , black dash curve). In addition, applying the SET CCL is suggested as the control procedure to modify the filament to switch in one of two stacking layers. Figure5 includes the details of mechanisms of the filament geometry modulation and thermal effect under low/high SET CCL. Below1 mA, the filament diameter growing with increasing CCL leads to switching gap migrating from high-k to low-k layers[98,73]. The filament is heated up with high SET CCL i.e. 1 to 5 mA and the NL decrease due to lowering dielectric constant of

the filament at high temperature[99, 100]. It has been found that thicker high-k layer in the stacks generally requires higher current (e.g. 2 mA for the H11S2 device) to obtain certain nonlinearity (> 10). In other words, the thickness ratio of high-k and low-k layer needs to be optimized in order to achieve the desired nonlinearity under low CCL region (<1 mA).

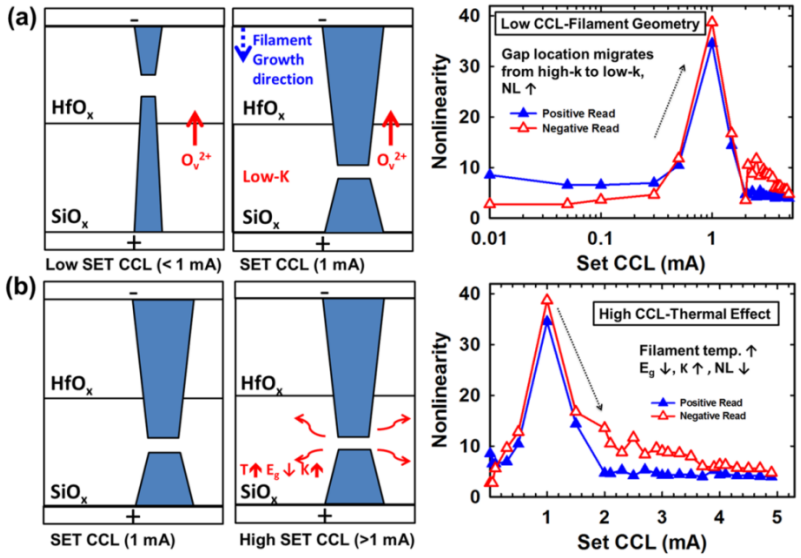



Figure 3.5. (a) Schematics of SET CCL effect on NL and filament RS gap migration from high-k to low-k oxide materials in low SET CCL range (<1 mA) leads to high NL, (b) schematics of SET CCL effect on NL and thermal effects of switching layer in high SET CCL range (>1 mA) causing NL dropping.

### 3.3.4. Seasoning effect in Oxide-based RRAMs

To investigate the stability of selectorless devices, Figure 6 shows the examination process for low-k layer quality determination by analyzing forming and 1st RESET processes in detail ($HfO_x$ (4 nm)/ $SiO_x$ (9 nm) structure as an example). The I-V characteristics with high electroforming voltage and leaky post-forming resistance (Figure 3.6 (a)) did not result in the nonlinear characteristics as compared to the I-V

characteristics with low electroforming voltage and resistive post-forming resistance one Figure 3.6 (b)). The nonlinearity with cycles, high-voltage current, and low-voltage current are investigated. This indicates that the potential hard breakdown induced by higher voltage forming process is undesired for the nonlinearity and selectorless device reliability. Note that the devices with low forming voltage have resistive post-forming resistance (read at -0.5V), and the 1st RESET process show a sharp nonlinear increasing region from the low-voltage response, named as "sharp increase" region on current transport behaviors.

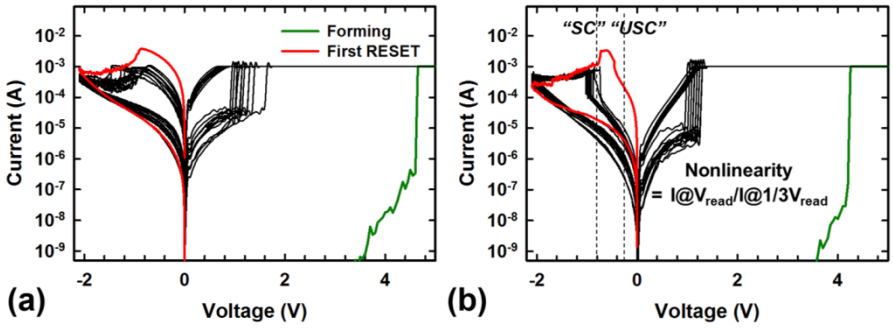



Figure 3.6. (a) I-V characteristics, high electroforming voltage, 1st RESET, and later switching process, and (b) I-V characteristics, low electroforming voltage, 1st RESET, and later switching process. All results are measured from H4S9. "SC" and "USC" named selected cell current and unselected cell current.

Figure 3.7 compares two cases mentioned in Figure 3.6, namely, the inefficient seasoning and the efficient seasoning. Inefficient seasoning is a condition for which it takes extensive amount of time to achieve nonlinearity due to leaky of 1/3 read region. For efficient seasoning, nonlinearity is quickly approached to stable state driven by to resistive of 1/3 read region, i.e. suppressed low-voltage current and high nonlinearity. Note that more robust low-k layer with less forming process damage can determine the

nonlinearity and selectorless device reliability and stability under the fixed SET current compliance limitation (SET CCL=1 mA). In other words, the device-to-device (D2D) variation results from the early stage operation e.g. electroforming and first RESET should be considered even followed by the identical operation schemes. The four cases are included for the relationship between the 1st RESET and the seasoning performance i.e. nonlinear 1st RESET (green arrow (i-ii)) and linear 1st RESET (blue arrow (iii-vi)). Figure 3.7 (b) shows the statistics of the correlation between the 1st RESET and nonlinearity. The strong seasoning correlations have been presented for the case (i) and case (vi), which including 20 devices for H7G5 and 20 devices for H4S9 bilayer stacked structures have been tested. Chu et. al. have also observed similar phenomena of charge quantity is the critical factor for forming process[101]. The over-forming would lead to device damage i.e. hard breakdown as well as increasing the quantity of charge through the switching layer. The formation of the conducted path can be mitigated by the ultrafast pulse electroforming further to form a discontinuous conduction path in the low-k layer and better nonlinearity.

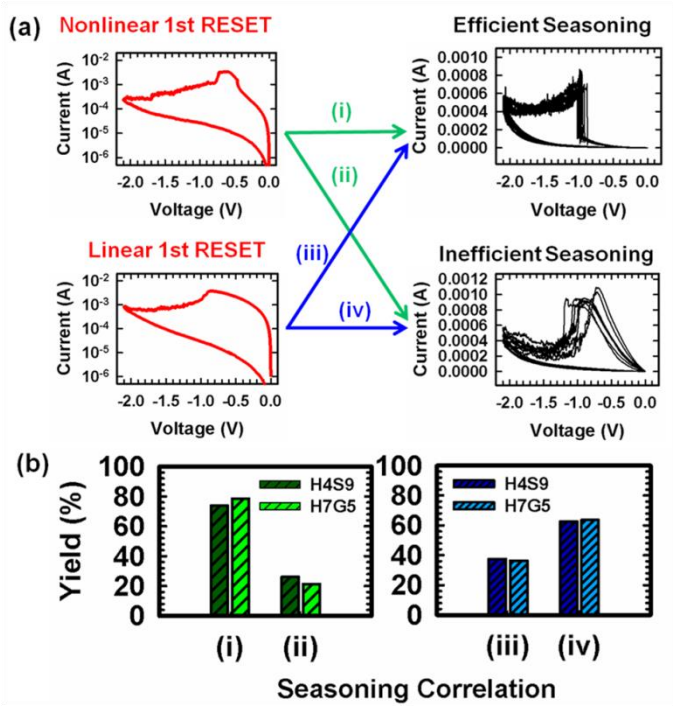



Figure 3.7. (a) Nonlinear first RESET and seasoning cycles on nonlinearity i.e. efficient and inefficient seasoning (i & ii); linear first RESET and seasoning cycles on nonlinearity i.e. efficient and inefficient seasoning (iii & iv) based on V/3 read scheme. (b) Yield of four modes for selectorless RRAM seasoning implementations.

Current in the high-voltage region (-0.5 V) exhibits different characteristics than current in the low-voltage region (named “sharp increase” behaviors) (See inset of Figure 3.8 and Figure 3.6 (b)). Transport in this voltage range is found to fit well to the Fowler-Nordheim (F-N) tunneling formula (red region and zoom-in plot of Figure 3.8 inset) with scientifically accepted accuracy (R2 =99%), which showed that less overshoot damage in lower forming voltage may induce Fowler–Nordheim (F-N) tunneling, as compared to which with higher forming voltage devices. The results also confirm that the seasoning effect is related to nonlinearity improvement by robust low-k layer quality and less forming process damage can improve the nonlinearity and selectorless device reliability.

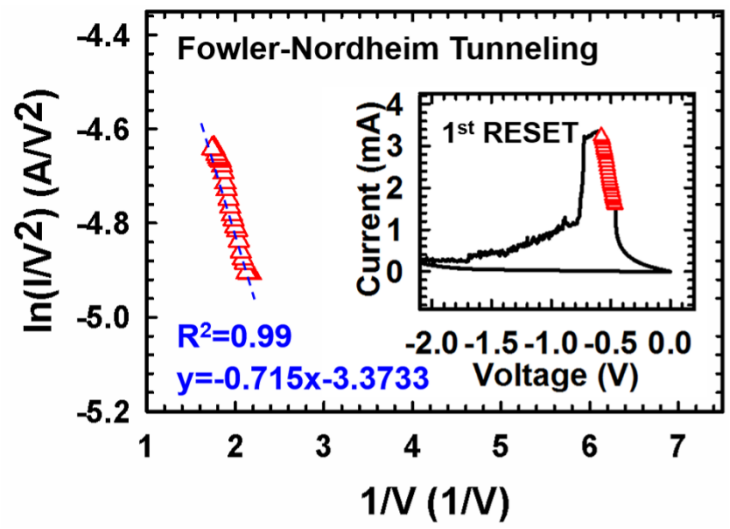



Figure 3.8. Fowler-Nordheim (F-N) tunneling fitting in the high voltage region of efficient cycling as seasoning cycles on the selectorless memory device. (Inset shows the 1st RESET I-V characteristics and fitting region).

### 3.3.5. Ambient effect in Oxide-based RRAMs

Figure 3.9 shows the HRS, LRS, and on/off ratio of $SiO_x$-based and HfOx-based devices through ambient switching experiments. The first 30 DC cycles are conducted in the air and followed by 30 DC cycles in the vacuum. There are five devices of $SiO_x$ (2 nm) been measured and demonstrated the sensitivity to ambient changes; five devices of $SiO_x$ (10 nm) been tested with no sensitivity to ambient changes. This depicts that the "non-robust" or "weak" filament formation in 2 nm $SiO_x$ layer, which results in the sensitivity to ambient changes. In addition, 10 devices for each different $HfO_x$ integrated structures were tested, i.e. $HfO_x$ (4 nm)/$SiO_x$(9 nm), $HfO_x$(11 nm)/$SiO_x$ (2 nm), $HfO_x$ (11 nm), and the ambient change immunity is confirmed in each device with good repeatability. Before the ambient testing, 30 RS DC cycles were performed after electro-

formation to stabilize the conductive filament, eliminate early-failures, and other reliability issues prior to the ambient test. As discussed in the previous section, the on/off ratio is smaller in 2 nm $SiO_x$ device than in 10 nm single $SiO_x$ layer devices is suggested as the non-robust filament formation. Figure 3.9 (a) shows the 10 nm single layer $SiO_x$ device exhibits 2 orders of magnitude on/off ratio for the first 30 cycles in air, and 1 order of magnitude on/off ratio for 2 nm $SiO_x$ single layer device. However, the spontaneous shrinkage of on/off ratio cannot be ignored under vacuum for 2 nm $SiO_x$ devices, with a clear transition during the sequential ambient changes. A simultaneous response to ambient switch i.e. the 31 DC cycle in 2 nm $SiO_x$ single layer device is thought to provide a higher surface-to-volume ratio, as compared to the 10 nm device which exhibits no responses. Based on the HRS current, 2 nm $SiO_x$ single layer device shows more than 1 order increment (i.e. window closure in the vacuum, re-open as back to air, data not shown). On the other hand, there is no ambient response observed in the $HfO_x$ single layer devices (Figure 3.9 b, top). Interestingly, the HRS increases as ambient changing while the LRS remains steady in $SiO_x$ single layer, suggesting that the conducting filament becomes more conductive and difficult to re-oxidize under vacuum due to lack oxygen concentration in dielectric layer[102]. The switching behavior reappeared immediately when bringing the $SiO_x$ devices back into the air (data not shown). The higher sensitivity towards ambient change showed in $SiO_x$ single layer is attributed to the highly sensitive characteristic of Si filament than the Hf conductive filament. As a comparison, HfOx single layer and $HfO_x/SiO_x$ stacked devices measured through the identical environmental conditions shows the immunity to ambient changes, as showed in Figure 3.9 (b). This suggests that oxygen vacancy (defect) concentration is sufficient in the HfOx-based structures and is able to maintain the HRS with re-oxidation even under insufficient oxygen supply externally i.e. vacuum. Even though the on/off ratio and the

switching voltages did not exhibit significant differences in the single layer HfOx device, the lack of nonlinearity makes it less desirable for crossbar array applications due to the sneak path issue. Thus, the $HfO_x/SiO_x$ bilayer device has been demonstrated to achieve a higher on/off ratio (~$10^2$), a desirable built-in nonlinearity, and low RS voltage (~1 V), meanwhile with superior immunity to ambient switches.

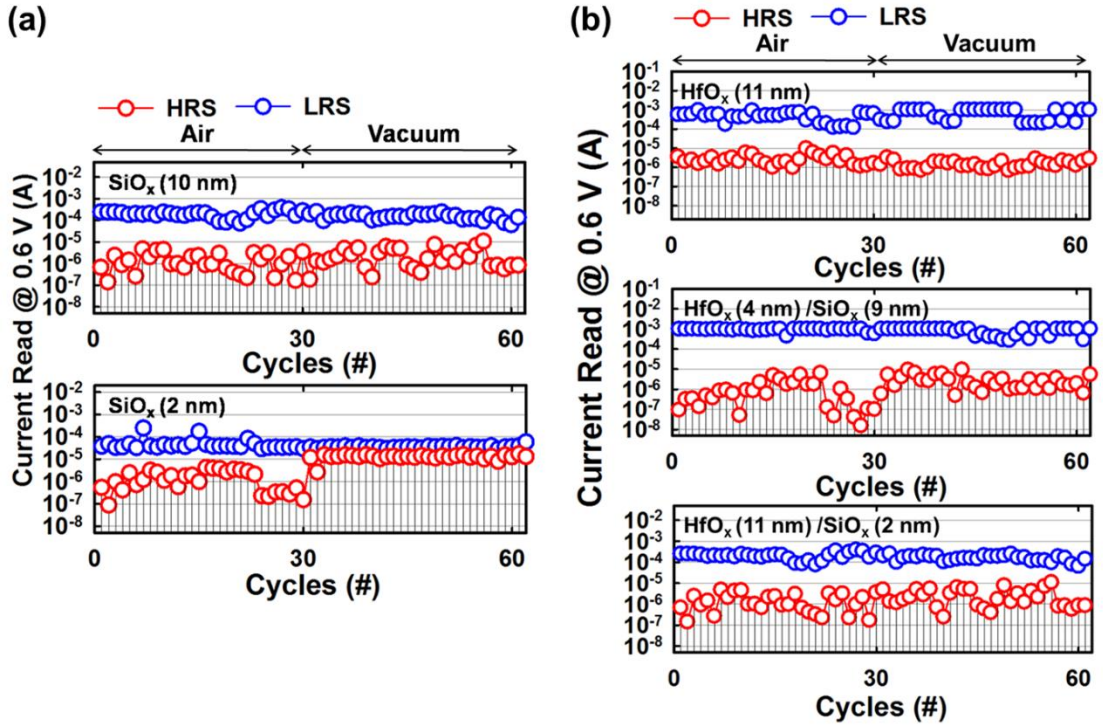



Figure 3.9. DC cycles with air-vacuum switches on (a) $SiO_x$ (10 nm) and $SiO_x$ (2 nm) single layer devices, (c) $HfO_x$ (11 nm), bilayer $HfO_x$ (4 nm)/$SiO_x$ (9 nm) and $HfO_x$ (11 nm)/$SiO_x$ (2 nm) devices.

Figure 3.10 shows the resistive switching voltages of 30 cycles in the air (i.e. grey box) and 30 cycles under vacuum (i.e. pink box) for all of the five structures. It depicts that the bilayer structures exhibit a superior immunity of ambient changes i.e. inserting the $HfO_x$ layer as an oxygen reservoir, which helps to avoid the switching voltage

degradation (Figure 3.10). As pulling the vacuum to 2.5 mtorr, SET voltage shows no differences within all the structures with operating in air. However, RESET voltages under vacuum enlarged ~47% and ~84 % in the 2 nm and the 10 nm $SiO_x$ single layer devices, possibly due to $H_2O$ and oxygen evacuation out of the dielectric layer and RESET occurs at the higher voltages. In other words, Si conductive filament (CF) becomes stronger in the vacuum (i.e. hard to RESET) with not sufficient oxygen provided. This is suggested that the formation of nano-porous structures in the $SiO_x$ film through the sputtering deposition, i.e. moisture and oxygen are easy to be absorbed/desorb from environment to the materials/materials to environment. On the other hand, the RESET voltage decreased ~29% for $HfO_x$ single layer devices operated in the vacuum, which indicates the Hf-CF is not be affected by the externally manual oxygen evacuation process owing to intrinsic stronger microstructure with high oxygen concentrations[103, 104].

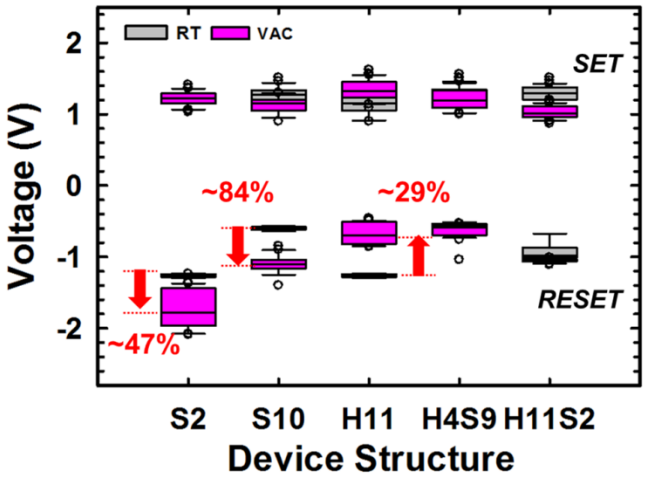



Figure 3.10. Switching voltages of single layer $SiO_x$, $HfO_x$ and bilayer structures, tested in the air (black plot) and under vacuum (pink plot).

Table 3.2. Comparison of switching characteristics and parameters in ambient effect on RRAM devices.

| Structure | | Ionic liquid (Electrolyte)/ $TiO_x$/ Pt[27] | Ag/ $Ta_2O_5$/ Pt [23] | Cu/ $Ta_2O_5$/Pt [28] | Cu/$SiO_x$/Pt [29-30] | This work | |
|---|---|---|---|---|---|---|---|
| | | | | | | Pt/$SiO_x$/TiN | Pt/ $HfO_x$ /$SiO_x$/TiN |
| Type | | VCM | VCM | VCM | ECM | VCM | VCM |
| Resistive Switching (RS) | SET | +5 V | +0. 5 V | +2 V | +2~+2.5 V | +1.2 V | +1.1V |
| | RESET | -5 V | -0.7 V | -0.5 V | -1~-1.5 V | -1.1 V | -0.6 V |
| Ambient Effect on RS voltage | Air | N/A | N/A | Not affected | Low | Not affected | Not affected |
| | Vac. | Low | Higher $V_{SET}$; Not affected $V_{RESET}$ | Not affected | High | Not affected $V_{SET}$; Higher $V_{RESET}$ | Not affected |

To obtain a good ambient change immunity of RS behaviors (i.e. on-off ratio and switching voltages), the bilayer structure i.e. $HfO_x/SiO_x$ bilayer structures have been developed. By inserting an interface within resistive switching structure, the defect density increases within the switching layer as compared to the single layer devices[15,16]. The SET (~1 V) and RESET voltages (-0.6 V) are found to be independent on ambient changes in bilayer structures, which is believed to be due to the higher oxygen density provided by $HfO_x$ layer. Table 3.2 summarizes the ambient effects on different oxide RRAM devices, including $TiO_x$, $Ta_2O_5$ and $SiO_x$-based RRAMs with varied electrodes. A low voltage (<1 V) operation with superior nonlinearity and ambient immunity of RS behaviors has been achieved in this study by using the $HfO_x/SiO_x$ stacked structures.

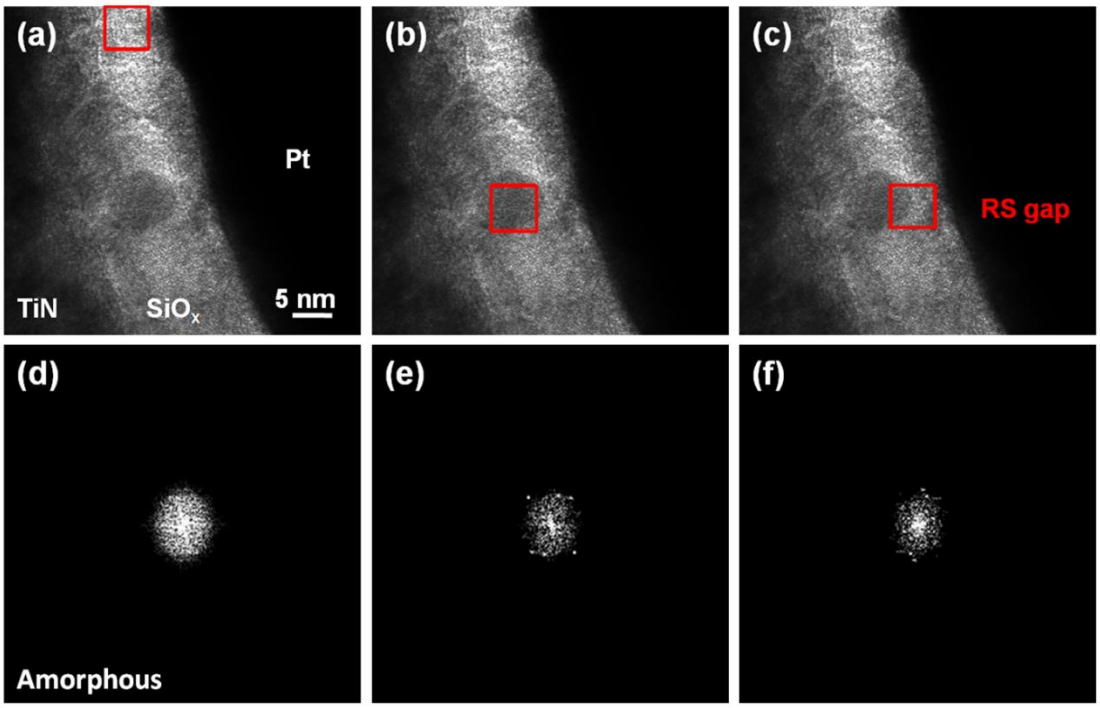



Figure 3.11. (a-c) TEM cross-section image of Pt (top electrode, TE)/$SiO_x$ (10 nm)/TiN (bottom electrode, BE) RRAM; (d-e) X-ray diffraction pattern for non-filamentary region, filamentary region and RS gap region.

In order to confirm the Si filament and the sensory gap, the microstructure analyses are conducted. The silicon filament is observed through transmission electron microscope (TEM) as the additional evidence of conductive pathways observation of Si-rich filamentary (i.e. instead of Hf metal filament) in $SiO_x$ RRAM devices, which attribute to the "sensory region" through the resistive switching behaviors. The microstructure analyses with switching site of the SiOx single layer device was prepared by focused ion beam (FIB), and examined by TEM and selected area pattern (SAD) as shown in Fig. 11. Si nano-filaments (NFs) were observed with the RS gap (red box region, Figure 3.11 (b) and (c)), which did not exist in non-filamentary regions indicating the amorphous structure is observed (Figure 3.11 (a)). The lattice spacing of the crystalline structures with the filament (Figure 3.11 (e)) and the RS gap (Figure 3.11 (f))

are 0.25 and 0.19 nm, corresponding to a Si (200) and a Si (022) plane by the ESVision software[105]. This is thought to suggest that the electroforming process breaks the Si-O bonds to form Si-Si bonds which then form the Si NFs through local crystalline structural changes after 30 DC switching cycles. The switching is correlated to Si NFs embedded in SiOx dielectric layer, where $SiO_x$ served as the source of Si pathway formation as followed the current flow direction. With the actual visualization of the switching pathway, the size of Si NFs (d < 5 nm) allows the scaling for ultra-small localized switching more feasible. The phenomenon where $SiO_x$-based switching with ~ 1 V SET occurs in air ambient without any backward-scan effect is thought to arise from conventional filament-type formation-rupture mechanisms in the RS gap regions. Accordingly, the additional capping HfOx layer with Hf-encapsulation apparently provides the source of oxygen in the vacuum, which passivates the ambient sensitivity of $SiO_x$ layer. Clearly, $HfO_x/SiO_x$ stacking optimization maintains the RS behaviors in the vacuum without the fatal programming window closure and avoids the resistive switching voltage degradation. Meanwhile, the improvement in nonlinearity by inserting the SiOx-layer can be used to implement selector-less large-scale array applications.

### 3.4 CONCLUSION

A built-in non-linearity of the bilayer oxide-based one-resistor (1R) device was proposed and experimentally achieved without an additional diode or a selector, where the device exhibited desirable NL characteristics to suppress current at low voltage region in opposite to regular $HfO_x$-based or $SiO_x$ single layered RRAMs. Also, the I-V curves were fitted to understand the transport mechanisms and to investigate the effective dielectric constant and RS region in stacking $HfO_x$-based RRAM devices. On the basis of

the observations, the bilayer stacked selector-less RRAM device can be not only used for preventing sneak path currents in cross arrays but also is a promising candidate for low voltage operating selector-less RRAM applications.

# Chapter 4: Graphite-based Selectorless RRAM with Improvable Intrinsic Nonlinearity for Array Applications

## 4.1 INTRODUCTION

A selectorless graphite-based resistive random-access memory (RRAM) have been demonstrated by utilizing the intrinsic nonlinear resistive switching (RS) characteristics, without additional selector or transistor for low-power RRAM array application. The low effective dielectric constant value (k) layer of graphite or graphite oxide is utilized, which is beneficial in suppressing sneak-path currents in crossbar RRAM array. The tail-bits with low nonlinearity can be manipulated by the positive voltage pulse, which in turn can alleviate variability and reliability issues. The results provide additional insights for built-in nonlinearity in 1R-only selectorless RRAMs, which are applicable to the low-power memory array, ultrahigh density storage, and in-memory neuromorphic computational configurations.[3]

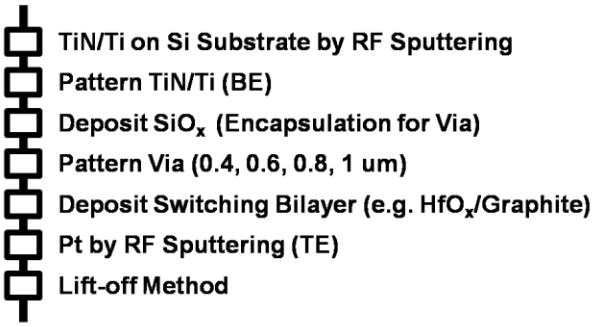
## 4.2 DEVICE DESIGN AND FABRICATION

### 4.2.1 Graphite-based RRAM device fabrication

RRAM devices with various side lengths of 400 nm, 600 nm, 800 nm, and 1 μm have been fabricated. The starting substrates were heavily-doped N+ Si wafers. Titanium nitride (TiN) of 200 nm was deposited as the bottom electrode. Then, 5, 8, 10 nm of

[3] The content of Chapter 4 is published in Ying-Chen Chen, Szu-Tung Hu, Chih-Yang Lin, Burt Fowler, Hui-Chun Huang, Chao-Cheng Lin, SungjunKim, Yao-Feng Chang, and Jack C. Lee, "Graphite-based Selectorless RRAM: Improvable Intrinsic Nonlinearity for Array Applications", Nanoscale (2018) The author is contributed in design of experiments, sample fabrication and characterization, manuscript writing.

graphite and followed by 7 nm of $HfO_x$ were deposited as resistive switching dielectric layers for bilayer structures by radio frequency (RF) sputtering. Note that graphene produced from RF sputtering deposition inevitably possesses defects such as grain boundary and wrinkles that may provide an oxygen pathway and alter properties of the film. Furthermore, graphite oxide was formed after $HfO_x$ deposition (discussed in the later session). Platinum of 165 nm was then deposited as top electrodes, as followed by lift-off process for RRAM devices. The $HfO_x$ (11 nm) single layer devices and $HfO_x$ (4 nm)/$SiO_x$(9 nm) bilayer devices areused as references. The abbreviations for the single layer (e.g. H11) and bilayer device structures (e.g. H7G5, S7G5) are listed (Figure 4.1). An Agilent B1500 and Lakeshore probe station were used for electrical characterization of the RRAM devices.




| Switching Layer Abbreviation | $HfO_x$ (nm) | $SiO_x$ (nm) | Graphite (nm) |
|---|---|---|---|
| H7G5 | 7 | 0 | 5 |
| S7G5 | 0 | 7 | 5 |
| H4S9 | 4 | 9 | 0 |
| H11 | 11 | 0 | 0 |

Figure 4.1. Fabrication process for bilayer selectorless RRAMs, and the summary table of bilayer structures (i.e. H7G5, S7G5, H4S9) and $HfO_x$ single layer structure as reference.

The sneak path current ($I_{sneak}$) through unselected neighboring cells is a major

problem in crossbar RRAM array configurations, which significantly affects the read operation and accuracy. To address the sneak path current issue, a transistor or a selector device is typically integrated with the memory device. Unfortunately, integrating an additional selector device, i.e. 1T-1R and 1S-1R configurations, considerably increase the manufacturing complexity and cost while limiting the scalability. In order to reduce the process complexity and cost for future microelectronic scaling, the selectorless 1R-only RRAM are proposed for suppressing the sneak path current without utilizing a selector device (Figure 4.2).

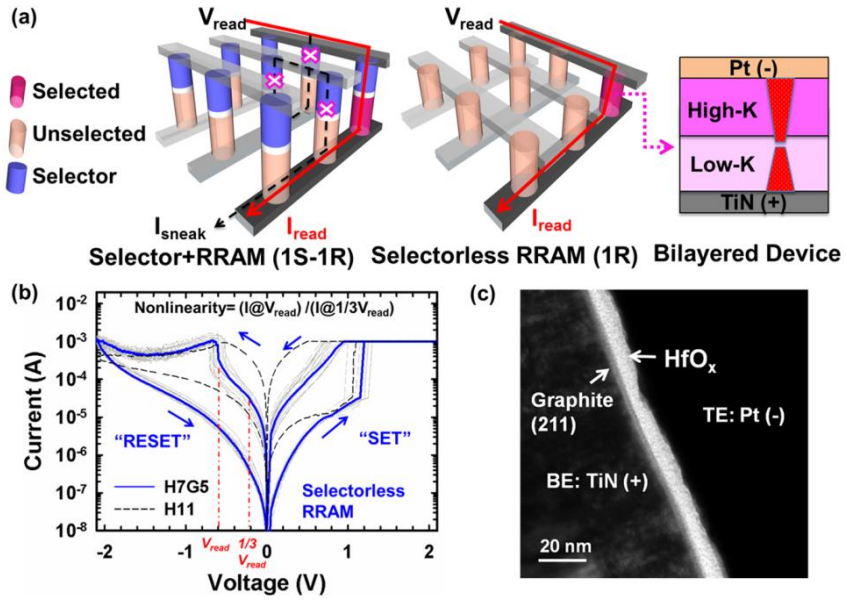



Figure 4.2. (a) Schematics of regular 1 selector +1 memory (1S-1R) configuration, 1R selectorless RRAM, and the dielectric constant bilayer design for selectorless RRAM, (b) I-V characteristics of bipolar RS operation in HfOx single layer RRAM and selectorlessHfOx (7 nm)/graphite (5 nm) stacked RRAM (H7G5), (c) TEM image for HfOx (7 nm)/graphite (5 nm) stacked devices.

### 4.2.2. Material analysis

Figure 4.3. (a) shows the transmission electron microscopy (TEM) image of H7G5 stacked device, and the graphite in the crystallographic plane of (211) is examined by X-ray diffraction (XRD) (Figure 4.3 (b)). Figure 4.3 (b) shows the energy dispersive X-Ray spectrum (EDX) line scan results of the H7G5 device. The offset between Hf and O peaks with broaden oxygen spectrum are observed. This depicts the oxygen penetration and graphite oxide (GO) formation after $HfO_x$ film is deposited. Meanwhile, as-deposited graphite in a (221) crystalline plane has been examined by the X-ray diffraction pattern (Figure 4.3(b)), which is in the rhombohedral structure. The C-V characteristics of graphite oxide have been measured, and the k-value of graphite oxide was found to be approximately 3.01. The result is similar to the values have been reported in the literature[106-108]. Figure 4.3 (b, inset) illustrates a possible model of resistive switching localized gap in the H7G5 bilayer structures. The NL gap modulation method by tuning the SET CCL in high-k/low-k stacked structures is also applied on graphite-based RRAMs.

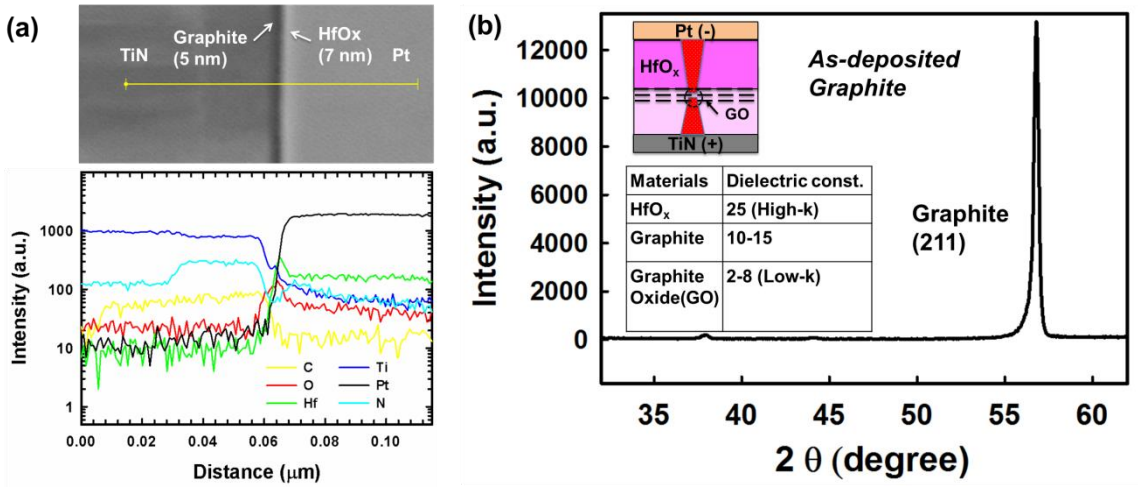



Figure 4.3. (a) The TEM image of H7G5 devices and the EDX line scan taken along the indicated yellow lines of the Pt/$HfO_x$/graphite/TiN, (b) XRD patterns of graphite (211) crystalline phase with as-deposited graphite layer.

## 4.3 CHARACTERIZATION

### 4.3.1 Graphite-based Selectorless RRAM with intrinsic nonlinear characteristics

The typical bipolar resistive switching I-V characteristics during DC voltage sweeps for the H11 and H7G5 bilayer selectorless RRAM devices (Figure 4.4). Voltage was applied to the bottom electrode (TiN) with the top electrode (Pt) connected to ground, and DC sweeps after electroforming process ($V_{forming}$~3.5 V for H7G5; ~4 V for H4S9; ~5 V for S7G5). The nonlinearity (NL) is defined as the current at high voltage i.e. $V_{read}$, divided by the current at low voltage i.e. 1/3 $V_{read}$ in V/3 read scheme. In other words, the sneak path current can be avoided by taking advantage of nonlinearity in the self-rectifying I-V characteristics i.e. low resistance state (LRS) of 1R selectorless RRAM itself.

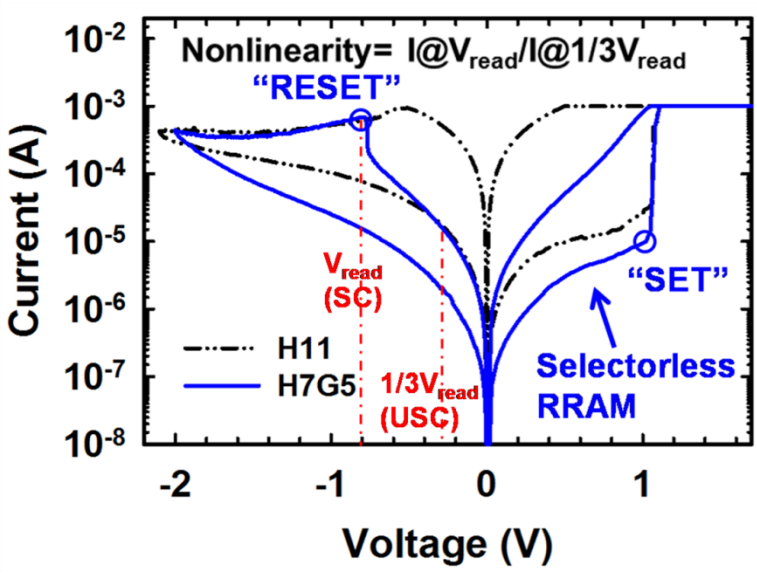



Figure 4.4. Typical I-V characteristics of bipolar resistive switching (RS) operation in $HfO_x$ single layer RRAM (H11, black dash line), and bilayerstackedselectorless RRAM (H7G5, blue line). The Vread applied on selected cell (SC) and 1/3Vread applied on unselected cell (USC) for suppressing the sneak path current in array configuration.single layer RRAM (H11, black dash line), and bilayerstackedselectorless RRAM (H7G5, blue line). The Vread applied on selected cell (SC) and 1/3Vread applied on unselected cell (USC) for suppressing the sneak path current in array configuration.

The C-V characteristics of graphite oxide have also been measured, and the k-value of graphite oxide has been measured approximately as 3.01, which is utilized as a low-k dielectric layer in bilayer selectorless RRAM. The higher nonlinearity is observed in bilayer stacks in "high-k/low-k design" (i.e. H7G5, H4S9) as compared to "low-k/low-k" (i.e. S7G5) and $HfO_x$ single layer RRAM. Noted the 30 cycles are included in cycle-to-cycle (C2C) variability and 20 devices measured for device-to-device variability (Figure 4.5).

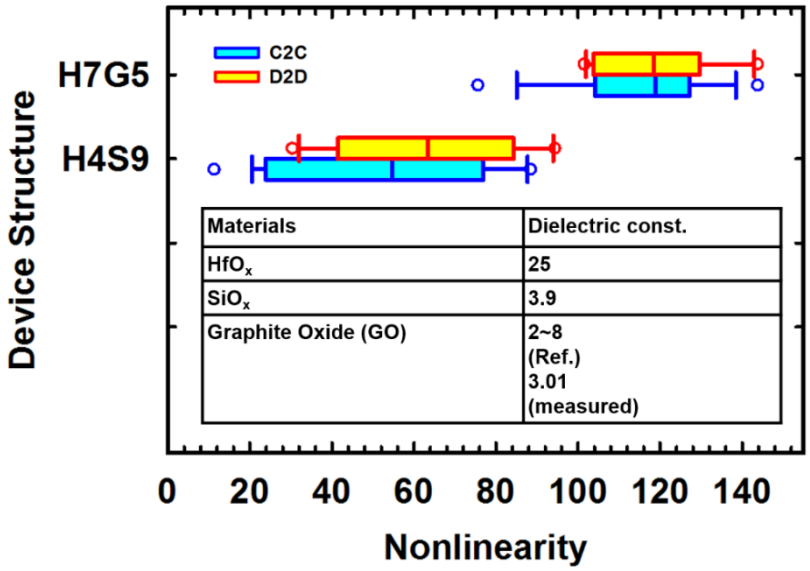



Figure 4.5. The nonlinear nature of bilayer stacks in "high-k/low-k design" (i.e. H7G5, H4S9) and low nonlinearity of "low-k/low-k" (i.e. S7G5), and HfOx single layer RRAM. The 30 cycles included in cycle-to-cycle (C2C) variability and 20 devices measured for device-to-device variability.

The gap design method by SET compliance current limit (CCL) during the SET process has been reported in chapter 3, and applied to the H11 and H7G5 device under voltage sweep operation. The operation window with good nonlinearity is observed between 0.6 mA and 3.2 mA for H7G5 device by V-sweep operation (Figure 4.6). A plausible mechanism can be expressed into two parts i.e. filament geometry and thermal effect. As the SET CCL increases, the filament width becomes wider and the switching gap migrates from high-k layer to low-k layer resulting in higher NL. As the SET CCL further increases i.e. up to 3.2 mA, the temperature increases due to higher currents causing the lower effective bandgap, higher k-value, then leading to lower NL. Besides, the current sweep operation enlarges the operation window with accessible nonlinearity (~40) and maintained as CCL up to 5 mA.

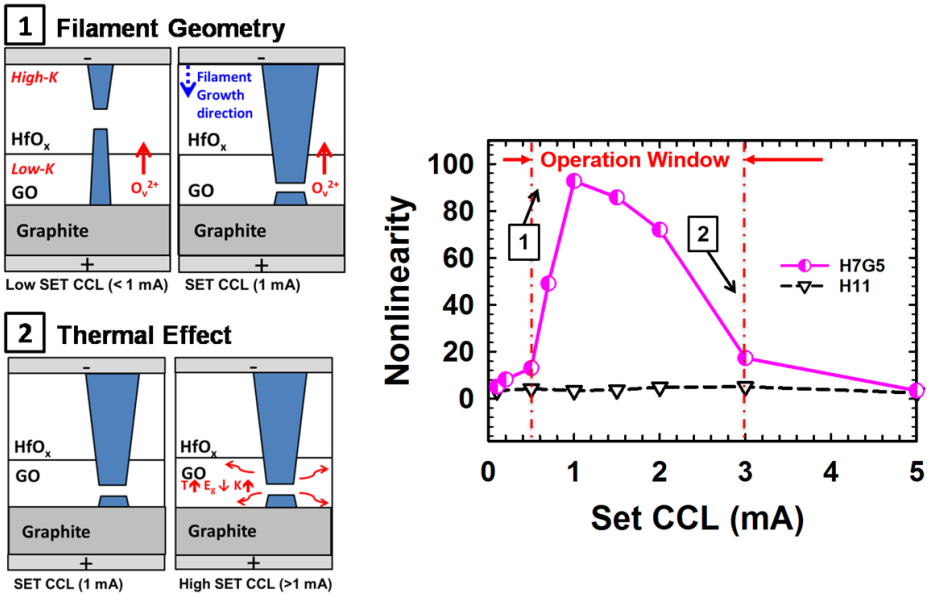



Figure 4.6. Mechanism of gap design method includes two parts i.e. filament geometry and thermal effect. SET CCL increases, the filament width becomes wider and the switching gap migrates from high-k layer to low-k layer resulting in higher NL. As the SET CCL further increases, the temperature increases, the effective bandgap decreases, k-value increases, NL increases.

Table 4.1. Comparison of switching characteristics and parameters of graphite-based resistive devices

Comparison of switching characteristics and parameters of graphite-based resistive switching devices.

| Device stacks | Deposition method | Switching polarity | Switch type | Thickness | SET | RESET | On/off Ratio | Nonlinearity |
|---|---|---|---|---|---|---|---|---|
| Pt/GO/Ti/Pt | Vacuum Filtration | Bipolar | Interface | 8 nm | 3.5 V | -3.5 V | $<10^3$ | - |
| Cu/GO/Pt | Vacuum Filtration | Bipolar | Filamentary | 15 nm | 1 V | -0.8 V | <10 | - |
| Al/GO/ITO | Hummers method | Bipolar | Filamentary | 30 nm | 2 V | -2 V | $<10^3$ | - |
| Ag/GO/ITO | Spin-coating | Unipolar | Filamentary | 30 nm | -1 V | -0.5 V | $<10^4$ | - |
| Au/CrGO/ITO | Hummers method | Unipolar | Filamentary | 30 nm | 5 V | 5 V | $<10^3$ | - |
| Al/GO/Al | Hummers method | Bipolar | Filamentary | 10 nm | 2.5 V | -2.5 V | $<10^2$ | - |
| Cu/a-C/Al | Sputtering | Bipolar | Filamentary | 200 nm | 2 V | -2 V | <10 | - |
| **Pt/$HfO_x$/G/ TiN (This work)** | **Sputtering** | **Bipolar** | **Filamentary /Interface (Area dependent)** | **<5 nm** | **1 V** | **-1 V** | **$10^2$** | **> 60** |

The recent reports on graphite-based resistive switching devices are summarized in Table 4.1. Only a small number of resistive switching devices were deposited using the sputtering deposition method to demonstrate the resistive switching behaviors i.e. switching voltage, polarity, and on-off ratio. Most of the graphite-based devices used chemical-involved Hummers methods[109, 110], which are not as compatible for CMOS processing. The switching voltage of the H7G5 of ~1 V is beneficial for low-power applications. Moreover, this work has reported the nonlinear nature (NL> 60) of graphite-based materials as a choice for selectorless RRAM devices to solve the sneak path current issue in high-density memory array applications.

### 4.3.2. Device-to-device (D2D) and cycle-to-cycle (C2C) variability

The cumulative probability distribution of nonlinearity in 3-cycling-segment i.e. 1-10 cycles, 11-20 cycles, and 20-30 cycles after electroforming on the H7G5 device is shown in Fig. 7 (a). The larger cycle-to-cycle (C2C) variation (median of 10 devices) in 1-20 cycles as compared to 21-30 cycles is observed. This suggests that the filament is under sculpturing and needs more DC cycles for performance stabilization.

With cycling increases, NL is increased as for the "seasoning effect." More experiments need to be conducted in future work for understanding the mechanism. The H7G5 structure has demonstrated a good nonlinearity and maintaining NL of 40~60 for 200 DC cycling operations. The reliability characterization, e.g. endurance, and the underlying mechanism are being investigated. The set pulses play a similar role as the DC seasoning cycles, while relatively gentle. In industry, pulses are utilized to stabilize the device performance such as HRS and LRS etc. The nonlinearity increases from 20 up to 50 within 30 DC cycles after forming. The decrement of current at $1/3V_{read}$ i.e. increasing the NL after seasoning cycles is observed, and the self-selective nature in I-V characteristics (after 30 DC seasoning cycles).

Although the selectorless RRAM is achieved by bilayer stacking with varied dielectric constant design, the device-to-device (D2D) variation is observed. The tail-bits are defined as whose NL is lower (< 20) as the outlier within the RRAM array after electroformation, which is probably due to the deposition uniformity and the slight misalignment with choice of SET CCL (Figure 4.7(b)). In other words, the "low NL tail-bits" inevitably exist while using the bilayer stacking engineer for selectorless RRAMs.

Note that the term “tail-bits” are the outlier bits where the nonlinearity is lower, after electroformation. Figure 4.7(b) shows the D2D variation with area dependency in the H7G5 selectorless RRAMs. In order to improve the nonlinearity of the tail-bits, positive pulse voltage modes are proposed and demonstrated in the following section.

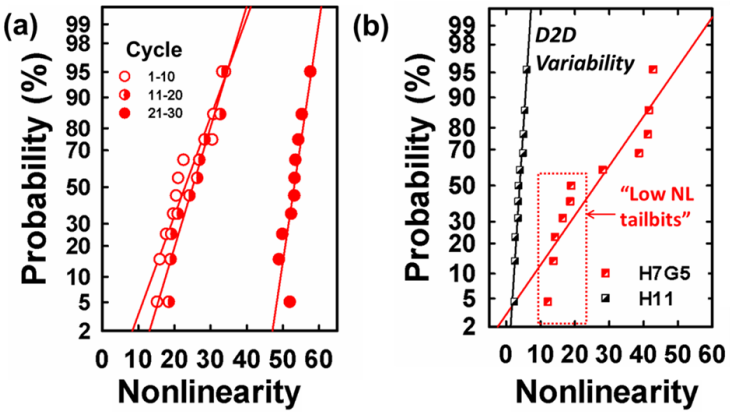



Figure 4.7. (a) Cumulative probability distribution of nonlinearity in 3-cycling-segment (i.e. 1-10 cycles, 11-20 cycles, and 20-30 cycles) of the H7G5 device, (b) device-to-device (D2D) variation of H7G5 with relative “low NL tail-bits” and H11 (left), and device area effect of H7G5 device (right).

### 4.3.3. Improvable intrinsic nonlinearity by pulse modulation

The low-nonlinearity cells as the tail-bits resulting in variability of the RRAM array applications (blue cell in the schematic in Figure 4.8 (a)) can be improved by applying set voltage pulses with specific pulse waveform in mapping the pulse height, pulse width, and pulse numbers. Two modes have been used as the refine-sculpturing process, i.e. with (mode 1)/without (mode 2), DC SET process. After the electroforming, the devices have been SET/RESET swept 30 cycles with SET CCL of 1 mA to roughly stabilize the switching gap, and then followed by the set pulses and a negative DC sweep to HRS for refine-sculpturing (i.e. gently widen the filament width) to migrate the

switching gap to low-k layer for improving NL. There are five devices with low NL characteristics were tested by adjusting the pulse height and pulse numbers; five devices with low NL were tested by adjusting the pulse width and pulse numbers for each positive voltage pulse modes. Based on the results, it seems that the low-NL cells as the tail-bits in the RRAM array applications (blue cell in the schematic in Figure 4.8 (a)) can be improved by applying set voltage pulses with specific pulse waveform, i.e. pulse height, pulse width. Thus, pulse operation can be used to fine-tune the filament shape and location (i.e. slightly larger filament width and move the switching gap to low-k layer for enhanced nonlinearity according to the derivation in chapter 2, Figure 2.3 (d). The nonlinearity is calculated in the negative polarity sweeps i.e. -0.28 V and -0.8 V. For mode 1, an additional SET process has been added before RESET to HRS, which ensures the filament is conductive in LRS and prevents the under-set situation (as a reference). Figure 4.8 (b) shows the NL mapping in pulse number (i.e. $10\sim10^3$) and pulse height (i.e. 1.5~2.4 V) under mode 1. Figure 4.8 (c) shows the same pulse number and pulse height under mode 2. As the pulses applied on the low NL tail-bit cell (deep blue), the NL was enhanced to ~80 (red) within the certain pulse height range (i.e. 2.0~2.2 V for mode 1; 1.6 ~ 2.0 V for mode 2 while independent on the pulse number. In other words, an additional DC SET process (i.e. “DC SET fuse”) results in the higher voltage pulse height is required in order to improve the NL of tail-bit cells. In this way, mode 2 is the focus for low power application as following. As applying these pulses on the high NL cell (NL> 60), the enhancement is not as significant as in the low NL cell while degraded with high pulse number (Figure 4.8 (d)), indicating the cell is “healthy enough” for the selectorless RRAM applications with well SET CCL control. With adjusting the pulse width and the pulse number, the low NL tail-bit is improved within the certain pulse width range (1 μs~1 ms), and independent on pulse number (Figure 4.8 (e)). If this pulse

applied on the high NL cell (Figure 4.8 (f)), the improvement is not significant while degrading with increasing the pulse number and pulse width, and showed the refine-sculpturing process is not required. The unique aspect of the positive voltage pulse mode is using pulses to gently widen the filament width, so to cause the switching gap to be located in the low-k layer for enhanced nonlinearity. The positive pulse with designed pulse height (e.g. 1.6 ~ 2.0 V) and pulse width (e.g. 1 μs~1 ms) provide a package of energy in a certain short time, and thus, the filament can be gently widened without overheating as a comparison to DC operations.

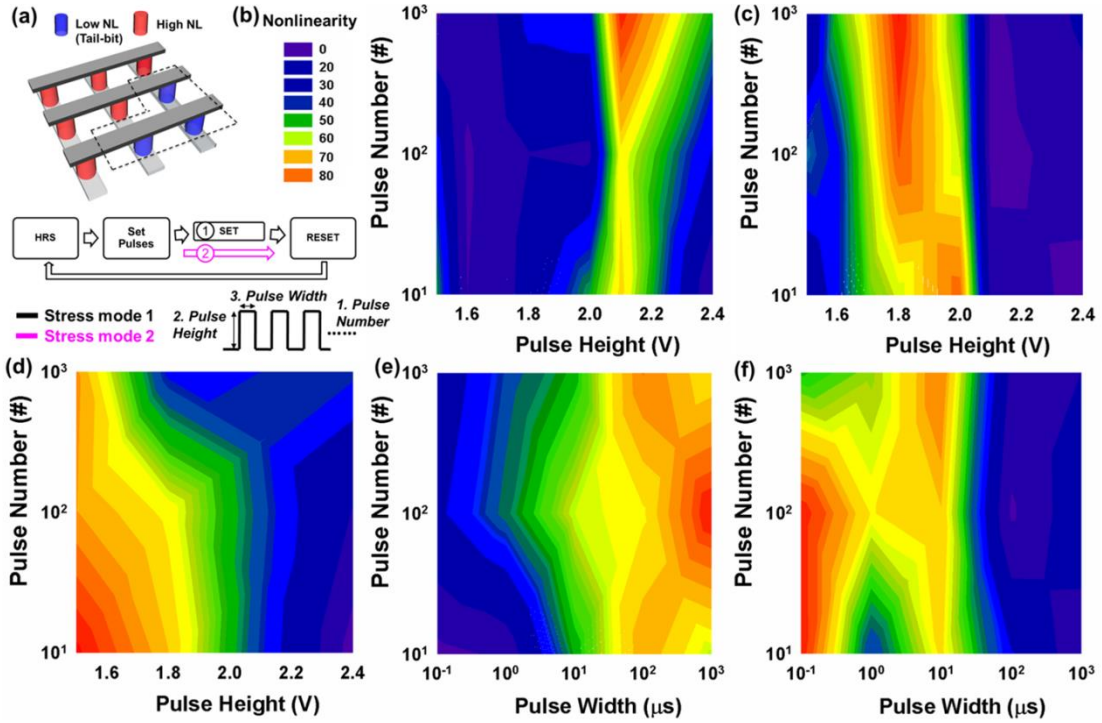



Figure 4.8. (a)Selectorless RRAM array with healthy NL cell (Red, NL > 60) and low NL tail-bits (blue in dash frame, NL< 20) under two positive pulse modes scheme (with and without "DC SET fuse", mode 1 and mode 2, respectively) for improving the tail-bits, (b) pulse height (1.6-2.4 V) with pulse number (10-$10^3$) starting with the low NL tail-bit (mode 1), (c-d) pulse height (1.6-2.4 V) with pulse number (10-$10^3$) starting with the low NL tail-bit and the healthy cell (mode 2), (e-f) pulse width (10-1-$10^3$ μs) with pulse number (10-103) starting with the low NL tail-bit and the healthy cell (mode 2).

### 4.3.4. Device area and thickness effect

In addition, the device size dependency is studied with measured values of MW and nonlinearity with various device structures (Figure 4.9). The nonlinearity has been found to be independent on the device sizes for various structures, which suggests the localized filament switching and the potential for high scalability on this bilayer selectorless RRAMs. The result shows the nonlinearity is independent on the device

sizes, which is thought to attribute to the filament switches in a narrow localization gap (~few nm).The nonlinearity and the number of possible word lines are higher in high-k/low-k stacked structures (i.e. H7G5, H4S9) than single high-k layer (i.e. H11) and low-k/low-k stacked (i.e. S7G5) structures.

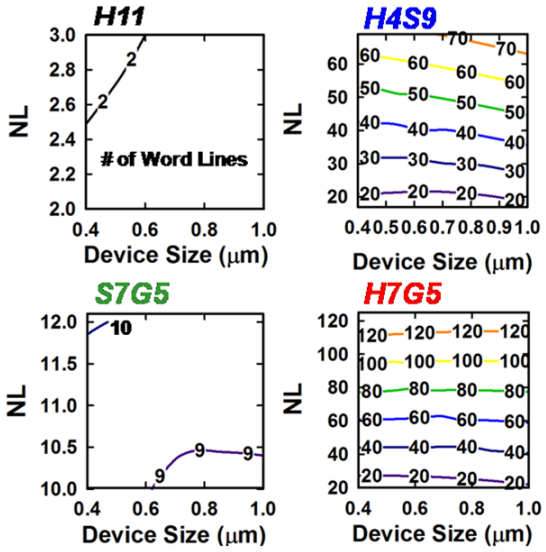



Figure 4.9. The crossbar array calculation based on measured NL and MW with various device sizes (0.4, 0.6, 0.8, 1 μm) on H11, S7G5, H4S9, H7G5 devices.

The thickness effect with various graphite thickness of 5, 8, 10 nm in $HfO_x$ (4 nm)/graphite stacks is investigated. The nonlinearity is independent on the thickess of graphite with the device-to-device variation of 20 devices (Figure 4.10). It suggested the GO formation after $HfO_x$ deposition is independent on the graphite thickness. In previous chapter, it shows the energy dispersive X-ray spectrum (EDX) line scan results of the H7G5 device. The offset between Hf and O peaks with broaden oxygen spectrum are

observed. This depicts the oxygen penetration and graphite oxide (GO) formation after $HfO_x$ film is deposited.

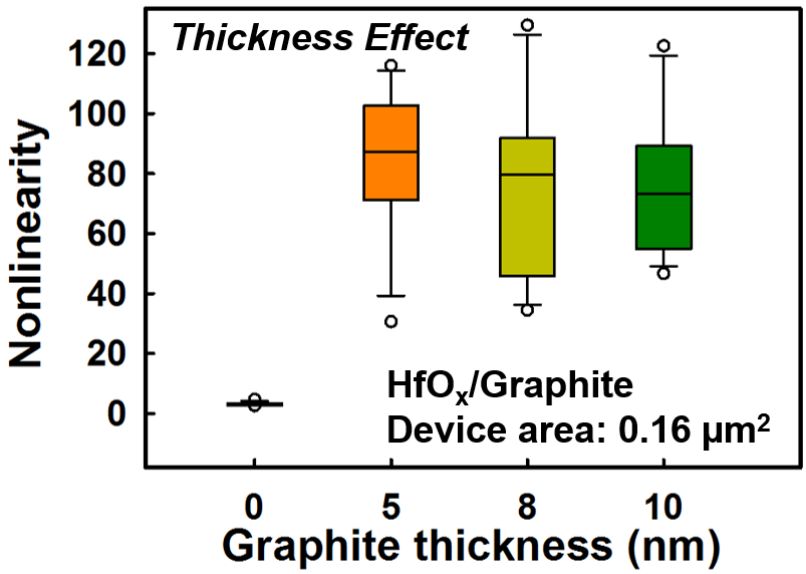



Figure 4.10. The measured NL as a function of various graphite thickness of 0, 5, 8, 10 nm.

The nonlinearity is optimized by modulating the SET CCL on the bilayer devices with low-k insertion layer, and the possible mechanism i.e. filament geometry modulation and thermal effect is provided. After the process is developed for fabricating the bilayer structures and the procedure for operating the devices, then the thickness ratio of high-k and low-k layer is further optimized to thereby improve the nonlinearity under low CCL condition (<1 mA). In other words, the thinner high-k layer would require lower CCL to obtain certain nonlinearity (> 10). The SET CCL effect read at -0.8 V is plotted, and nonlinearity reaches ~30 at CCL of 1 mA in $HfO_x$ (4 nm)/$SiO_x$ (9 nm). However, with the thicker high-k layer (e.g. H11S2), the higher SET CCL is required ~2 mA to obtain high

NL (~15) which is higher than in H4S9 (Fig. 11). In other words, the right shift of SET CCL with highest NL is observed. The inset shows the nonlinearity with device-to-device variation of H4S9 and H11S2 under SET CCL of 1 mA.

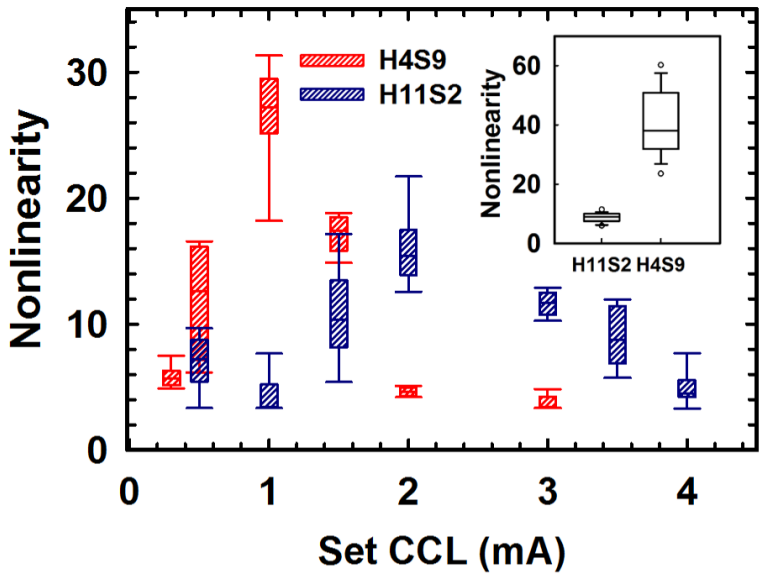



Figure 4.11. The nonlinearity of various oxide thickness stacks, i.e. H4S9, H11S2 devices.

### 4.3.2 Current Sweep (I-sweep) Method for Low Power Operation

The nonlinear nature of selectorless RRAM is investigated by voltage sweep (V-sweep), and current sweep (I-sweep) (Figure 4.12). The I-sweep operation provides the accessible nonlinearity with reduced high resistance state (HRS) current due to lower operation current with the suggested thinner filament.In other words, the switching power is suggested lower by utilizing the I-sweep method than V-sweep method. The nonlinearity is multilevel cell (MLC) is demonstrated on H7G5 selectorless RRAM by I-

sweep method. The interface defects in between two dielectric layers can be observed through I-V characteristic i.e. SET operation of H7G5 by I-sweep operation (dark pink), as compared to H11 with no material interface.

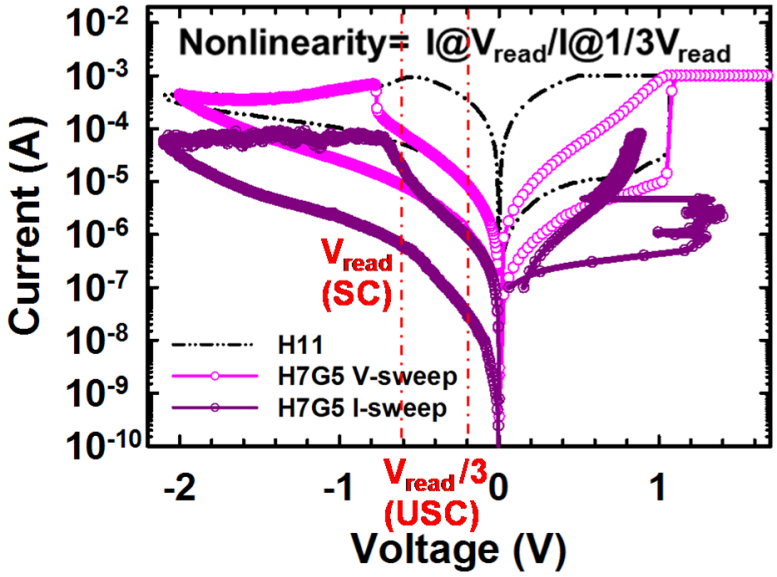



Figure 4.12. The I-V characteristics of two different SET operation modes on H7G5, i.e. voltage-sweep and current-sweep with the v-sweep for RESET.

On the other hand, the power consumption and energy efficiency are important for memory storage applications and in-memory computing configurations. The switching energy of various selectorless RRAMs in this work (Fig. 14, right panel) is compared with different emerging memory categories (Figure 4.13. left panel), i.e. phase change memory (PCM), magnetic random access memory (MRAM), NAND flash, and 1T-1R architecture using RRAM as memory element. The switching energy is reduced by utilizing the 1R-only bilayer selectorless RRAMs (i.e. ~40 pJ/bit of H7G5 by V-Sweep), which is ~4X lower than NAND flash and ~5X lower than PCM and 1T-1R configuration in comparison. In comparison of different operation schemes, the switching energy is further reduced by I-sweep operation (CCL=80 µA), which is ~2X lower than using V-sweep operation scheme on H7G5 device.

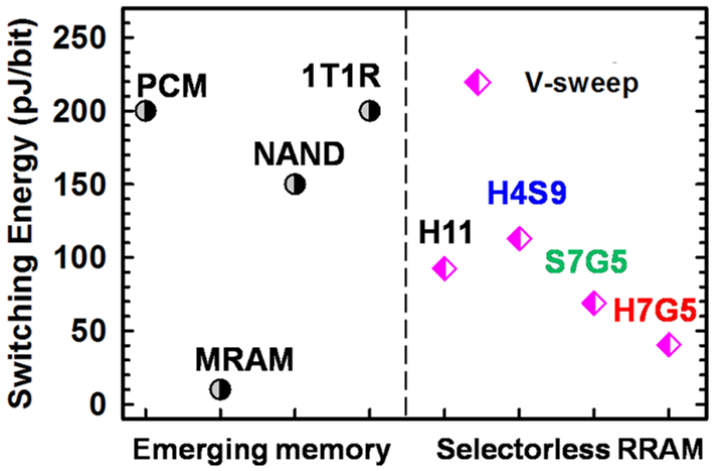



Figure 4.13. Switching energy comparison of device structures in this work on different emerging memory categories.

The benchmarks of bilayer selectorless RRAMs are summarized by nonlinearity as a function of memory window, switching voltages and energy (Figure 4.14) [111-116], showing that the H7G5 is an excellent candidate for bilayer selectorless RRAM with high nonlinearity (~120), good memory window (~$10^2$), and low switching energy (~40 pJ/bit).

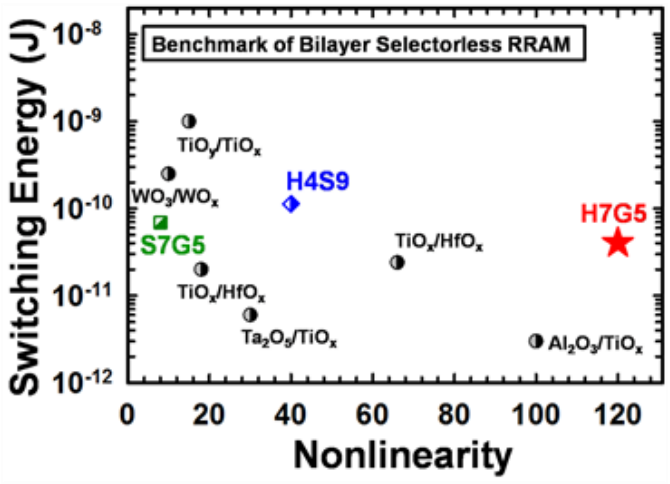



Figure 4.14. Benchmark of switching energy for current oxide-based bilayer selectorless RRAM devices.

## 4.4 CONCLUSION

In summary, the built-in nonlinearity characteristics have been realized by the graphite-based selectorless 1R-only RRAM without an additional diode/selector. The nonlinearity (~60) in the bilayer graphite-based RRAM devices has been demonstrated by controlling the SET compliance current limit (CCL). Besides, the NL is enhanced by a well-designed pulse waveform with pulse voltage scheme. The improvable nonlinearity characteristics of low-NL tail-bit are utilized in the bilayer device, which is desirable in

suppressing sneak-path currents in the low-power selectorless memory array, high-density storage, and neuromorphic processing.

# Chapter 5: Relaxation Characteristics and Resistive Switching Identification Methodology

## 5.1 INTRODUCTION

The RRAM with MIM structure is simplifying memory array design by crossbar architecture, however, the leakage through the sneak paths is inevitably induced while accessing this RRAM crossbar networks. The sneak paths current problem is one of the major issues in the development of three-dimensional (3D) crossbar memory designs. The sneak paths current (SPC) problem can be described as the leakage from neighboring unselected cells (USC), which results in significant the cross-talk and distorts the data of the selected cell (SC) during the reading operation. To mitigate the sneak paths currents, a diode or a selector device in series with a RRAM cell to form 1D-1R or 1S-1R structure has been developed[117-121]. Several solutions for selection devices including Mott transition switches, nonlinear volatile switches, threshold switches, rectifying diode devices etc. have been presented[122-126]. Unfortunately, the additional selection devices for 1S-1R configurations considerably increase fabrication process, circuit design complexity, and additional cost per chip. Therefore, a selectorless memory composed of 1R-only design architecture with nonlinear characteristics is desirable for high-density RRAM array applications.

In previous work, the selectorless RRAM in high-k/low-k bilayer stacks, in which the intrinsic nonlinearity has been demonstrated by inserting a low-k layer (e.g. $SiO_x$ layer or graphite oxide layer) and optimized by SET compliance current limit (CCL) modulation[127-130]. In addition, the bilayer or multilayer nonuniform metal-oxide-stacked structures for self-rectifying bahavior have been studied, e.g. $TiO_x/HfO_x$, $TaO_x/TiO_x$, $Al_2O_3/TiO_x$, $WO_3/WO_x$[111-116] etc. However, the mechanism of the nonlinearity-CCL

responses, and reliability characteristics are not yet been investigated. This work not only studied the reliability of relaxation characteristics under temperature variation, but also proposed a switching identification method which provides the potential guidance for future design of 3D sneak-path-constrained selectorless crossbar RRAM configurations.[4]

## 5.2 DEVICE DESIGN

The schematic of 3D crossbar 1S-1R array memory configuration is showed in Figure 5.1(a). Figure 5.1 (b) shows the transmission electron microscopy (TEM) image of bilayer $HfO_x/SiO_x$ stacked device. To initiate the resistive switching, a single voltage sweep electroforming process with a current limit was applied to induce a soft breakdown. After electroforming, the device manifests an improved conductance as the conductive filament (CF) connects the TE and BE, thus resulting in a low-resistance state (LRS) of the RRAM. The reset process can then be applied to rupture the CF, resulting in a high-resistance state (HRS). Then, the soft-breakdown process was performed by single sweeping the voltage until current abruptly increased to a compliance current limit (CCL) of 1 mA, as shown in Figure 5.1 (a). Voltage was applied to the bottom electrode (TiN) with the top electrode (Pt) connected to ground. By switching set and reset operations, the CF can be repeatedly connected/ruptured, and allowing reversible transition cycles between HRS and LRS. The SET process i.e. switching from HRS to LRS took place in positive polarity, while the RESET occurred in negative polarity.

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[4] The content of Chapter 5 is published in Ying-Chen Chen, Szu-Tung Hu, Chao-Cheng Lin, Jack C. Lee, "Resistive Switching Early Failure and Gap Identification in Bilayer Selectorless RRAM Applications" 77th Device Research Conference (DRC) (2019),
Ying-Chen Chen, Hui-Chun Huang, Chih-Yang Lin, Szu-Tung Hu, Yao-Feng Chang and Jack C. Lee "A Novel Resistive Switching Identification Method through Relaxation Characteristics for Sneak-path-constrained Selectorless RRAM application " (Under review) The author is contributed in design of experiments, sample fabrication and characterization, manuscript writing.

Figure 5.1 (c) shows bipolar resistive switching I-V characteristics during DC voltage sweeps for single $HfO_x$ layer (H11) and bilayer selectorless RRAMs (H4S9 and H7G5). The bipolar resistive switching I-V characteristics during DC voltage sweeps for single HfOx layer (H11) and bilayer selectorless RRAMs (H4S9 and H7G5). In this experiment, the total thickness of bilayer and single layer devices are designed to be ~11 to 13 nm, in order to reduce the influence of bias stress i.e. overset during the electroformation process. The extra bias stress though the forming process with potentially different shape of filaments is being avoided here. After the electroforming process, the resistive switching performance was stabilized by 30 DC voltage sweep cycles. The SET process for oxide-based RRAMs was performed by applying to 3 V forward/reverse double sweep with 1 mA CCL to program to LRS. The RESET process was done by sweeping up to -2.1 V, where current decreased as the voltage was swept from around RESET voltage, and the devices were then programmed into HRS. The nonlinear nature in selectorless RRAM is shown to mitigate the SPC because the LRS of selected cell can be read at a "high-voltage" region (i.e. -0.8 V), while the sharp conductance drops at "low-voltage region" (i.e. -0.4 V or -0.28 V) effectively suppresses SPC through unselected cells in reading schemes (e.g. V/2 or V/3 read schemes)[131,132]. In other words, the sneak paths current can be constrained by leverage the nonlinearity of the self-rectifying current-voltage characteristics. The nonlinearity is defined as the current at the read voltage ($V_{read}$) divided by the current at the one third read voltage (1/3 $V_{read}$) with V/3 scheme (half of read voltage (1/2 $V_{read}$) with V/2 scheme). The on-state of the selected cell (SC) is read at a "high-voltage" (i.e. $V_{read}$) region, while the sharp conductance decreases at "low-voltage region" (i.e. 1/3 $V_{read}$ or 1/2 $V_{read}$) effectively suppresses the sneak current through the unselected cells (USC). The nonlinearity of H7G5 (NL~120) stacked device exhibits ~24 times of improvement over that of H11

device (NL~5) with SET CCL of 1 mA, which suggests a significant increased current at Vread by inserting the high-k layer i.e. HfOx in bilayer devices, with reduced current at 1/3 Vread (~$10^{-5}$ A) for both structures. The high-k layer i.e. $HfO_x$ in H7G5 is shown to enhance the higher currents than those of H4S9 are around -0.8 V, where the same high-k layer and same SET CCL of 1 mA (i.e. switching gap in low-k layer) are utilized.

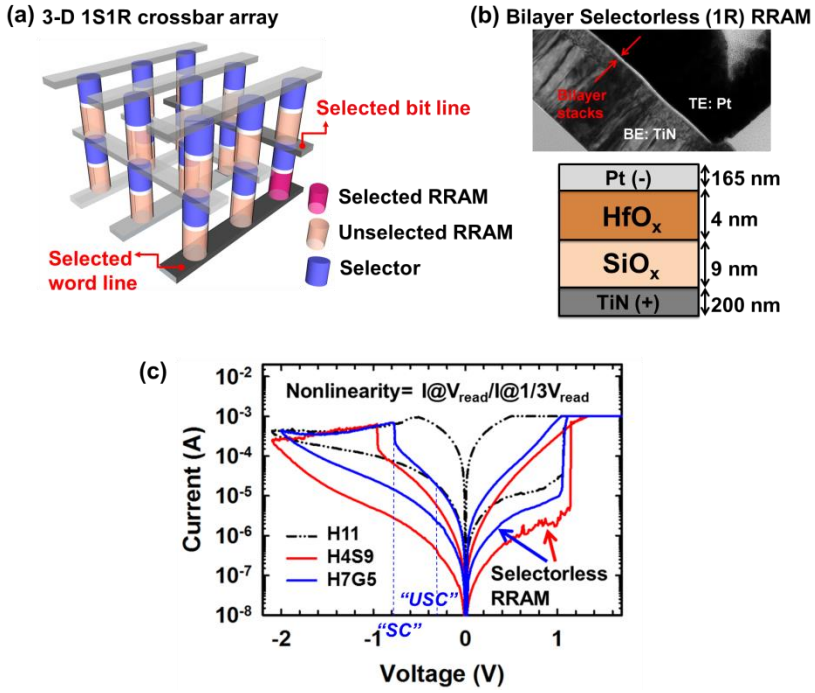


Figure 5.1. (a) Schematics of 1S1R crossbar array configuration for high class storage memory, (b) bilayer engineering structure design for selectorless RRAM with intrinsic nonlinearity in array applications, (c) I-V characteristics of $HfO_x$ RRAM (H11), 1R selectorless RRAM of $HfO_x$ (4 nm)/$SiO_x$ (9 nm) (H4S9) and $HfO_x$ (7 nm)/graphite (5 nm) (H7G5).

## 5.3 RESULTS AND DISCUSSION

### 5.3.1. Temperature Effect on Bilayer Selectorless RRAMs

The early failure yields are as 62.5%, 37.5%, and 7.7 % for H7G5, S7G5, H4S9, respectively, which depicts the H4S9 as having better DC cycling endurance than graphite-based selectorless RRAMs[133]. The number of word lines (N) assessment with nonlinearity by utilizing the V/3 read schemes are showed in Figure 5.2 (a), for single layer and bilayer selectorless RRAMs (median of 30 devices). The reading voltages are -0.8 V for fully read on selected cell, and -0.28 V for unselected cells. The bilayer devices i.e. H4S9 (or H7G5) have the nonlinearity of ~ 14 times (or ~18 times) higher than single layer device i.e. H11. After the calculation of array size by taking into account 10% read margin, the number of word line (i.e. the maximum array size) are 80 for H4S9 and 120 for H7G5, respectively. Although the H4S9 has slightly lower nonlinearity than H7G5, the early failure yield is also lower in H4S9 than in H7G5. In other words, there is a tradeoff between the reliability of memory window with the nonlinearity[133].

In addition, the nonlinearity readouts under various temperature conditions with SET compliance currents limit (CCL) modulation is shown in the Figure 5.2 (b). The results show thatthe nonlinearity properties are not affected by the ambient temperature under vacuum (~2.5 mtorr). The SET CCL modulation is applied under room temperature of 300 K, and 20 cycles for switching stabilization of each CCL condition are applied on devices. After DC cycles, the ambient temperature decreases from 300 K to 150 K, and the nonlinearity is characterized by V/2 scheme after the target temperature is reached for 5 minutes. The temperature elevation (i.e. 340 K, orange curve) is also applied and the nonlinearity shows slight decrements comparing to the cooling process, which is thought

to suggest that the thermal effect on filamentary structures decreases the bandgap and increase the effective dielectric constant resulting in nonlinearity decrement[134].

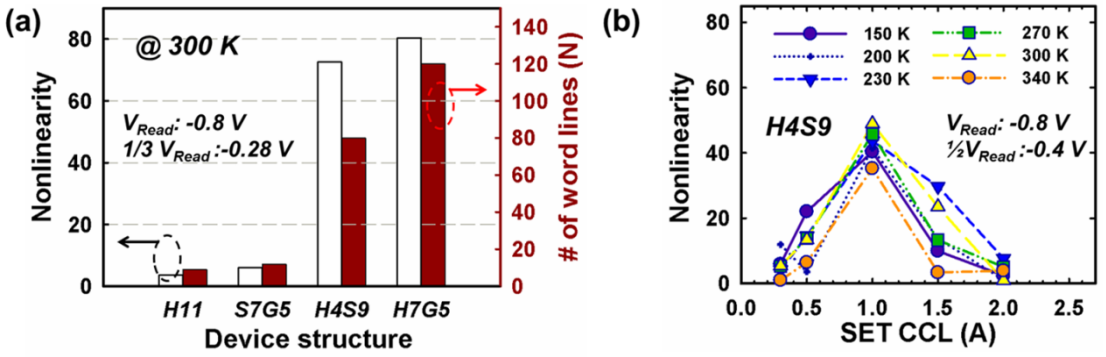


Figure 5.2. (a) Temperature effect of nonlinearity with SET CCL modulation on H4S9, (b) nonlinearity and calculated number of word lines (N) in various structures.

### 5.3.2. Relaxation Characterization

The relaxation characteristics of conductive filament with varied SET CCL of 0.1 mA and 2 mA for H11, S9, H4S9 (median of 10 tested devices for each structure) are compared and showed in Figure 5.3 (a). The normalized current (%) is defined as the current of time ($I_t$) divided by initial current ($I_0$) multiply by 100%. The current drift is the difference between two current percentages, i.e. $I_0$-It. Here, the current drift of 5% is chosen as a criterion to extract the activation energy. In other word, the time value utilized for Ea extraction is to have a 5% current drift (i.e. normalized current is 95%). The retention testing is applied every 60 seconds, and read voltage is 0.1 V. The results showed the current drift is larger as the SET CCL is lower in all the device structures, e.g. current drift ~5 % with CCL of 0.1 mA while <1% with CCL of 2 mA on S9 after 4000 seconds. This is thought to suggest that the conductive filamentary structure is thicker with higher SET CCL (e.g. 2 mA), which results in better retention and less current

drift[25]. On the other hand, the H11 showed the greater relaxation behavior (current drift ~2.5 %) in the comparison of H4S9 (current drift ~3.8 %) and S9 (current drift ~5%).

Figure 5.3 (b) shows the current drift as a function of time on S9 devices under various temperate conditions. With increasing temperature, the larger the filamentary structures relaxation occurs, ~11% under 393 K, ~8% under 358 K, ~5% under 333 K, ~4% under 298 K after 1 hour. Based on the observation of different relaxation behaviors with temperature on various devices, the methodology of switching identification is proposed (Figure 5.3(c)). The Arrhenius equation and extracted activation energy (Ea) are utilized, where the t is relaxation time under 5 % current drift, T is the ambient temperature (in kelvin) during retention testing, k is the gas constant of 8.314 x $10^{-3}$ (kJ $mol^{-1}K^{-1}$). By comparing the extracted activation energy value as an indicator, the information of filamentary structure composition and resistive switching can possibly be identified, which will be discussed in next session.

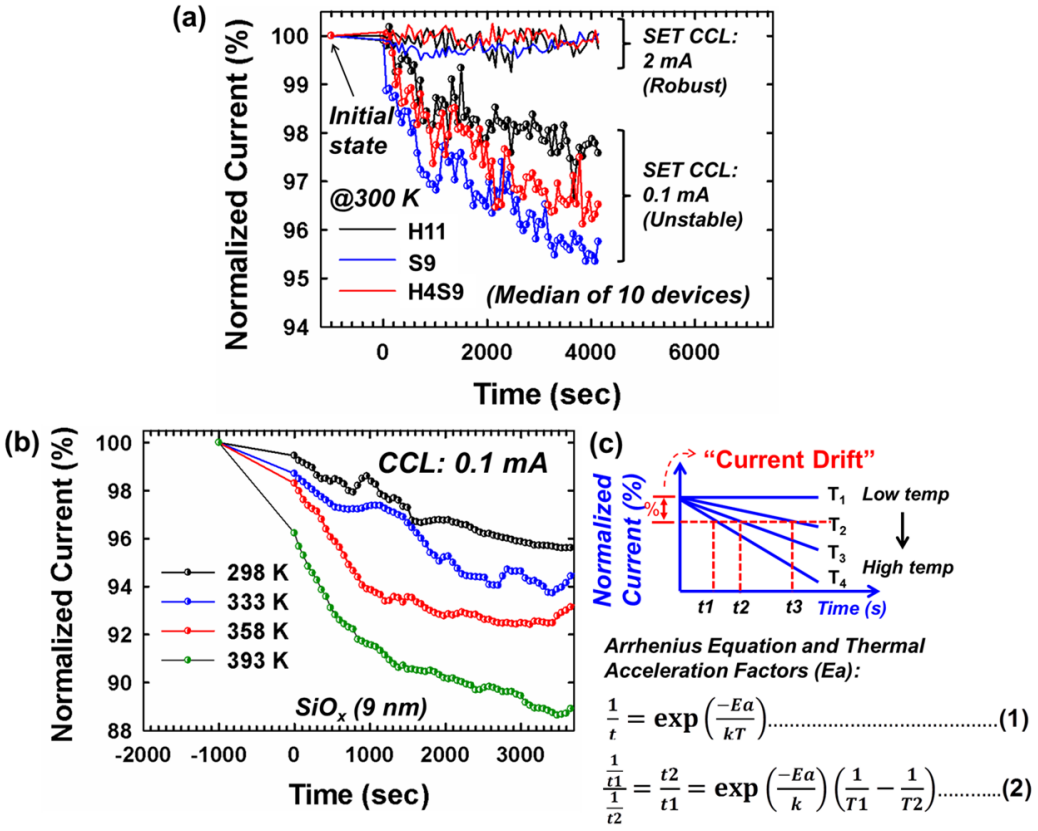


Figure 5.3. (a) The normalized current (%) change during filament relaxation with SET CCL of 0.1 mA and 2 mA under room temperature (black: H11, blue: S9, red: H4S9), (b) current reduction with temperature modulation of $SiO_x$ (9 nm), (c) activation energy (Ea) extraction methodology by relaxation behavior under various temperature conditions.

### 5.3.3. Acceleration Factor (Ea) Extraction

Table 5.1. Bonding energy, acceleration factor (extracted) and reaction rate for $HfO_x$ and $SiO_x$ single layers.

| | $HfO_x$ | $SiO_x$ |
|---|---|---|
| **Bond Energy (eV)** | **Hf-O: 8.16~8.43**<br>**Hf-Hf: 4.02** | **Si-O: 8.15~8.42**<br>**Si-Si: 3.2 eV** |
| **Activation Energy (Ea)** | **0.7~1.8** | **0.3~0.4** |
| **Relaxation Rate (τ)** | **Low** | **High** |

The extracted Ea values as a function of SET CCL with various temperatures are shown in Figure 5.4 (black curve for H11; blue curve for S9; red curve for H4S9). The temperatures of 300, 335, 360 K have been used in the retention measurements and relaxation behavior characterizations. The extracted activation energy (Ea) values based on Arrhenius equation are in the range of ~0.7 to 1.8 eV for single layer $HfO_x$, and ~0.3 to 0.4 eV for single layer $SiO_x$ (Figure 5.4, left panel). The extracted Ea values for H4S9 bilayer selectorless devices with SET CCL modulation is showed in Figure 5.4 (right panel). The preliminary result shows the nonlinearity characteristics of H4 and H11 with SET CCL of 1 mA are 3.08 and 3.04, respectively[132-134]. The nonlinearity is independent of the thickness of $HfO_x$ single layer devices, so the H11 as the reference sample to avoid extra voltage stress. Noted the Ea of $HfO_x$ (4 nm) is of ~1.87 eV at CCL of 1 mA, and not showing significant differences than $HfO_x$ (11 nm) (~1.67 eV). The extracted Ea value of H4S9 bilayer devices is in the median of ~0.32 eV as CCL is of 1 mA, and ~1.46 eV, ~0.7 eV, ~0.7 eV as CCL are of 0.1, 0.3, and 2 mA, which suggested that the resistive switching at SET CCL of 1 mA has Si and O ionized defects involved in the filament structures than other CCL conditions. The analysis of RESET process (i.e. filament

rupture process) is the based on the “hourglass model” as well as quantum point contact (QPC)[135, 136] model to present the oxygen vacancies or metal ions movements during switching process. Here, the relaxation behavior of filament utilized here for Ea extraction is also analyzed based on the hourglass model, where the thinnest part of conductive filament i.e. bottle neck is only composed of several metal atoms. During the relaxation process, the conductance of CF continues to decrease until fully ruptured the CF, where the metal filament dissolution process determines the process i.e. M-M bonds continue to break which requires less bond dissociation energy than M-O formation [42-43]. When the last atom is dissolved, the conductive filament is finally ruptured to HRS. Besides, the relaxation of Si-CF is faster than Hf-CF (Figure 5.3 (a)) which corresponds to the bond energy of Si-Si (~3.2 eV) is lower than Hf-Hf (~4.02 eV), while the bond energy of Si-O (8.15~8.42 eV) is similar to which of Hf-O (8.16~8.43 eV) (Table 5.1)[137,138]. In other words, the Si metal filamentary structure is comparably weaker than Hf metal filamentary structures which have higher Ea and lower reaction rate for LRS relaxation. The bond energy of Si-Si bond is ~20 % lower than of Hf-Hf bond, which explains the lower extracted Ea value showed in the SiOx single layer devices. According to Figure 5.2 (b) and Figure 5.4 (right panel), the H4S9 with SET CCL of 1 mA is showing the higher nonlinearity related to the Si filamentary structure than other CCL conditions, which depicts the optimized nonlinearity can be achieved by both modulating the CCL and insertion of a low dielectric constant layer.

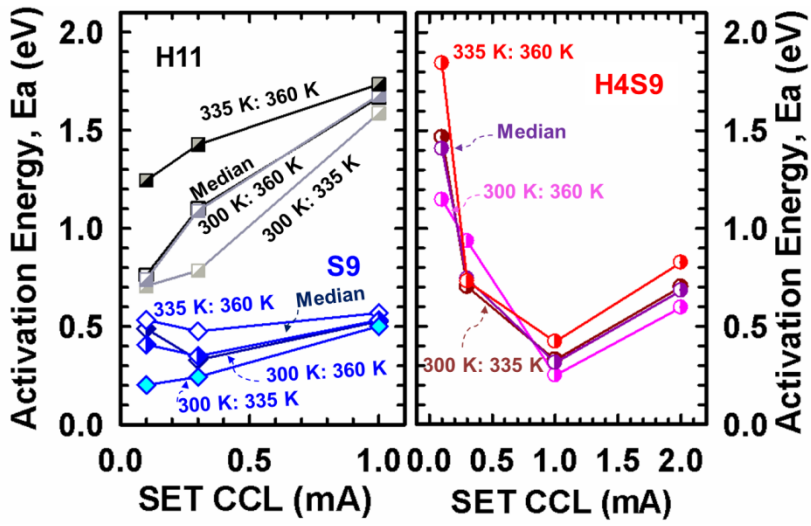


Figure 5.4. Activation energy (Ea) extraction methodology by relaxation behavior under various temperature conditions (black curve for H11; blue curve for S9; red curve for H4S9).

## 5.4 CONCLUSION

In conclusion, the intrinsic nonlinearity has been demonstrated in bilayer selectorless 1R-only RRAM without additional diode/transistor selector elements, which are beneficial in suppressing SPC in the high-storage-class crossbar memory array configuration. The resistive switching identification method utilizing reliability of relaxation properties, SET CCL modulation, and activation energy extraction have been reported, where the Ea is ~0.7 to 1.8 eV for single layer $HfO_x$, ~0.3 to 0.4 eV for single layer $SiO_x$, respectively. The relaxation characteristics and resistive switching identification provide the insights and mechanism understanding of bilayer selectorless 1R-only RRAM for high storage class crossbar memory configuration.

# Chapter 6: Read Margin of Selectorless RRAM for Crossbar Array Applications

Bilayer selectorless resistive random-access memories (RRAM) have been demonstrated by utilizing the intrinsic nonlinear resistive switching (RS) characteristics, without additional transistor or a selector integration. The bilayer structures i.e. high-k layer/low-k layer stacks are highly scalable, while suppressing the sneak path currents and reading error in crossbar RRAM array. The nonlinearity (NL) modulation is also investigated by different operating schemes. In this chapter, the numerical read margin calculated results provide additional insights intodevelopment and optimization of bilayer selectorless RRAMs with high nonlinearity (~120), good memory window (~$10^2$), and low switching energy (~40 pJ/bit), which enable the high- density storage, low-power crossbar array memory applications. In addition, the experimental results by read scheme is conducted on 2x2 crossbar array with varied sensing voltages.[5]

## 6.1 INTRODUCTION

To demonstrate the feasibility of solving the sneak-path issue by utilizing the observed self-rectifying behavior, numerical simulation of the maximum crossbar size and number of word lines (N) have been conducted. For an N × N crossbar array, the equivalent circuits using the one bitline pull-up read scheme (OBPU) approach and under the worst case scenario for reading a LRS cell or a HRS cell are utilized[139,140]. The worst

[5] The content of Chapter 6 is published in Y. -C. Chen, C. -Y. Lin, H. -C. Huang and J. C. Lee "Energy Efficient Operation Schemes of Nonlinear Selectorless RRAM for Crossbar Array Applications" 61st Electronic Materials Conference (EMC) (2019). The author is contributed in design of experiments, sample fabrication and characterization, manuscript writing.

scenario is where all unselected bits were at the low-resistance state with resistance of $R_{LRS}$.

## 6.2 NUMERICAL CALCULATION OF ARRAY APPLICATION

### 6.2.1. Equivalent circuit for read margin calculation

The read margin (RM) increases with the number of word lines (N) decreasing, which is owing to lower sneak path current through the unselected cells. The number of word lines i.e. array size is extracted on the premise of 10% read margin. The equivalent circuit of an N × N crossbar array for the one bitline pull-up read scheme is as shown in Figure 6.1. To program the 1S1R or selectorless crossbar array, a 1/3 $V_{read}$ voltage scheme[141,142], where full $V_{read}$ was applied on the selected cell and only 1/3 $V_{read}$ was applied on the unselected cells, can be utilized. As apparent in the nonlinear I-V characteristics, for a $V_{read}$ of 0.8 V, 1/3 $V_{read}$ less than 0.28 V was low enough to prevent program disturb. To read from the array under a worse case read scheme, which is the one bit-line pull-up scheme, was considered. In other words, only one bit line was pulled up, and all other bit lines were "floating" (no voltage applied) when each word line was selected. In addition, a worst case data pattern was assumed, where all unselected bits were at the LRS with resistance of $R_{LRS}$. The simplified equivalent circuit of a square N×N array with negligible line resistance is depicted in Figure 6.1[139,140].

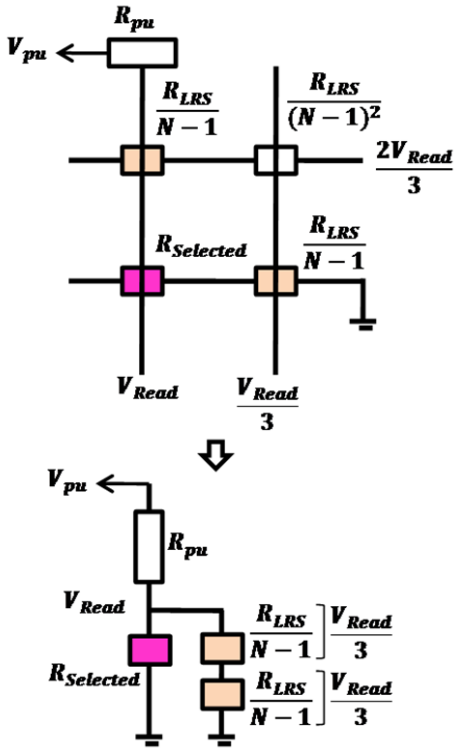


Figure 6.1. Equivalent circuit of an N × N crossbar array for the one bitline pull-up read scheme[2].

For a large array, the voltage across the parallel resistor network of the unselected word and bit lines (see $R_{LRS/(N-1)}$ in Figure 6.1) was only third of the voltage across the selected bit $V_{read}$. To a first approximation, $2R_{LRS/(N-1)}$ at $V_{read/3}$ through the sneak path should not be less than $R_{LRS}$ at $V_{read}$ to ensure a sufficient read margin between the high- and low-resistance states of the selected bit. In other words, the nonlinearity of the LRS in selectorless cells was the primary factor determining the maximum array size rather than the memory window between the high/low-resistance states (i.e. on-off ratio, $R_{HRS}/R_{LRS}$), which plays an important role in the optimization of the passive crossbar

array. The simulation of memory window related array size is conducted and discussed later.

A more quantitative assessment on the read margin $\Delta V$ normalized to the pull-up voltage $V_{pu}$ (i.e. $V_{read}$) can be calculated by solving the Kirchhoff equation where $R_{pu}$ is the resistance of the pulled-up resistor, set to $R_{LRS}$ at $V_{cell}$ for maximum voltage swing[139,140]. The assumption and derivation are as following:

$$\boldsymbol{R_{pu} = R_{LRS@Vread}}$$

$$\boldsymbol{\Delta V = V_{out,LRS} - V_{out,HRS}}$$

$$\boldsymbol{Read\ Margin}\text{: } \boldsymbol{\frac{\Delta V}{V_{pu}} = \frac{V_{out,LRS} - V_{out,HRS}}{V_{pu}}}$$

, and the Kirchhoff equation:

$$\boldsymbol{\frac{\Delta V}{V_{pu}}\ (N) = \frac{R_{pu}}{\left\{[R_{LRS}\ (V_{read})]||\left[\frac{2R_{LRS}\left(\frac{V_{read}}{3}\right)}{N-1}\right]\right\} + R_{pu}} - \frac{R_{pu}}{\left\{[R_{HRS}\ (V_{read})]||\left[\frac{2R_{LRS}\left(\frac{V_{read}}{3}\right)}{N-1}\right]\right\} + R_{pu}}}$$

The calculated maximum array size with at least 10% read margin improved from $N$ = 2 (RRAM without nonlinearity, e.g. H11) to $N$ = 120 (RRAM with nonlinearity, i.e. H7G5), where $V_{read}$ of 0.8 V was chosen not only to maximize NL but also to guarantee a sufficient margin of the read disturb. The calculated results suggest that the nonlinearity behavior itself can guarantee the N of 120 for H7G5, N of 80 for H4S9 on the premise of

10% read margin, which is improved in comparison to $HfO_x$ single layer devices (N=2) under the same read margin criterion (Figure 6.2).

$$\#\ of\ Word\ Lines = N, as\ \frac{\Delta V}{V_{pu}} \geq 10\%$$

Noted the read margin is around 50 % with the minimum array size (i.e. N=1) is under the assumption that $R_{HRS} >> R_{LRS}$ ($R_{HRS}$ domintes, $V_{out,\ HRS} \sim 0$). The read margin decreases with increasing the array size due to the more siginificant sneak path current contributed from neighboring cells. The intrinsic nonlinear nature of selectorless RRAM provided additional freedom in engineering nonlinearity by tuning the resistance of the RS element.

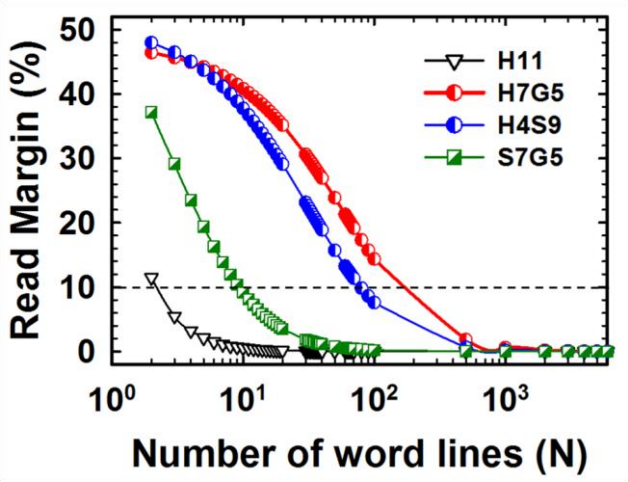


Figure 6.2. Read margin (%) as a function of N in various device structures. Number of word lines (N) is extracted by experimental results of I-V characteristics on H11, H7G5, H4S9, and S7G5 devices (via=0.4 μm), on the premise of 10% read margin.

### 6.2.2. Relation of read margin, memory window and nonlinearity

Figure 6.3 shows the simulated results of read margin (%) with various memory window (MW) at the fixed nonlinearity of 20. The read margin is suggested as dominated by the nonlinearity while is independent of MW once MW $>10^2$ (green, blue and navy curves).

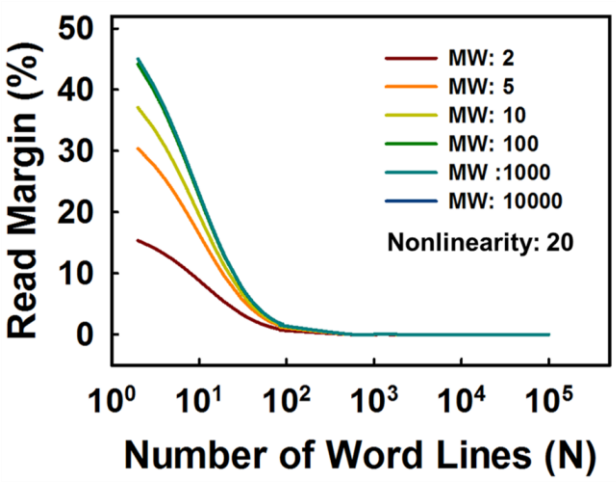


Figure 6.3. Simulated results with fixed NL (~20) with various MW (~2 to $10^4$). The read margin remains as the MW $>10^2$.

## 6.3 Experimental Results and Discussion

### 6.3.1 Device Fabrication

The RRAM 2x2 crossbar array with various side lengths of 400 nm, 800 nm, 1 μm and 1.2 μm have been fabricated. The starting substrates were N+ Si wafers. The 100 nm of $SiO_x$ is deposted by plasma-enhanced chemical vapor deposition (PECVD). Titanium nitride (TiN) (50 nm) was deposited as the bottom electrode by sputtering method. The $SiO_x$ of 450 nm is deposted by PECVD and patterned to form the via as followed by depositing the tungsten, chemical-mechanical polishing (CMP) process, and

fabricating the $Si_3N_4$ spacer. Then, 3 nm of $SiO_x$ and followed by 6 nm of $HfO_x$ were deposited as resistive switching dielectric layers for bilayer structures by radio frequency (RF) sputtering and atomic vapor layer (ALD) deposition, respectively. Titanium (20 nm) and TiN (30 nm) are deposited as top electrodes (Figure 6.4 (a) and (b)). The $HfO_x$ (6 nm) single layer device are fabricated as reference. The abbreviations for the single layer (e.g. H6) and bilayer device structures (e.g. H6S3) are used to stand for the device structures. The SEM image of 2x2 crossbar array structure is as showed in Figure 6.4 (c) (top view) and Figure 6.4 (d) (cross section view). An Agilent B1500 and Lakeshore probe station were used for electrical characterization of the RRAM devices.

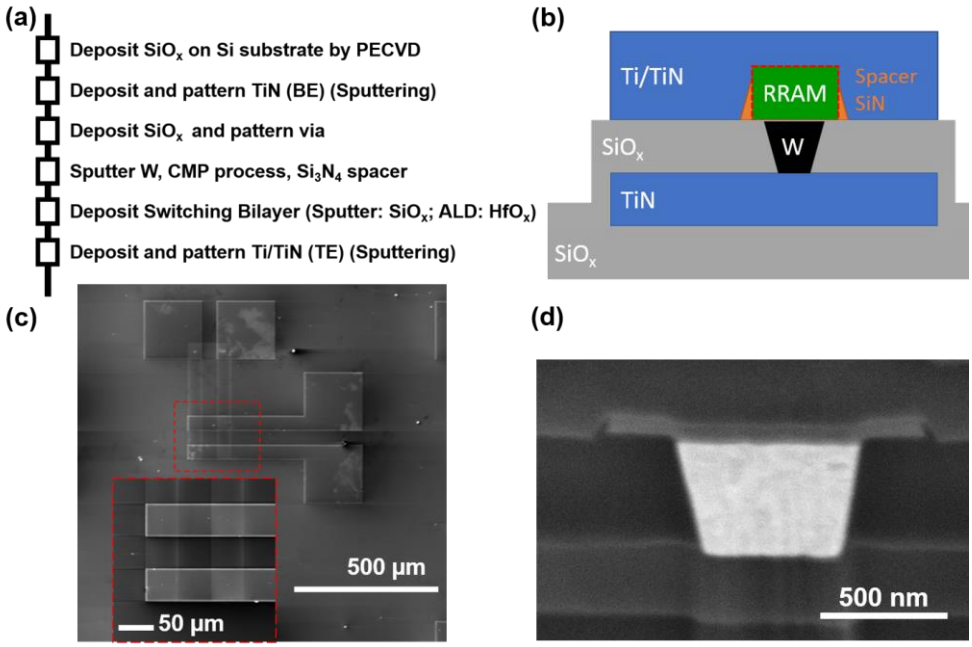


Figure 6.4. (a) Fabrication process for RRAM crossbar array, (b) schematic of one RRAM cell in crossbar array, (c) SEM image of crossbar array (top view), (d) SEM image of one RRAM cell in the crossbar array (cross section view).

### 6.3.2 RRAM crossbar array characterization

Figure 6.5. shows the experimental results of read margin on single layer and bilayer selectorless RRAM devices. The reading schemes and bias are applied as showed in the insets i.e. V/2 read scheme when the selected cell is under LRS (Figure 6.5 (a)) and under HRS (Figure 6.5 (b)) with various read voltage from 0.01 to 0.5 V. The read margin is degraded with increasing the read voltage, which is thought to be suggested the sensing current disturbances resulting from the bias stress. In addition, the read margin is higher in the H6S3 bilayer stacked device than H6 single layer device owing to the intrinsic nonlinear behavior of bilayer devices which improve the ability to suppress the sneak path current, to reduce the read error, and to improve the read margin.

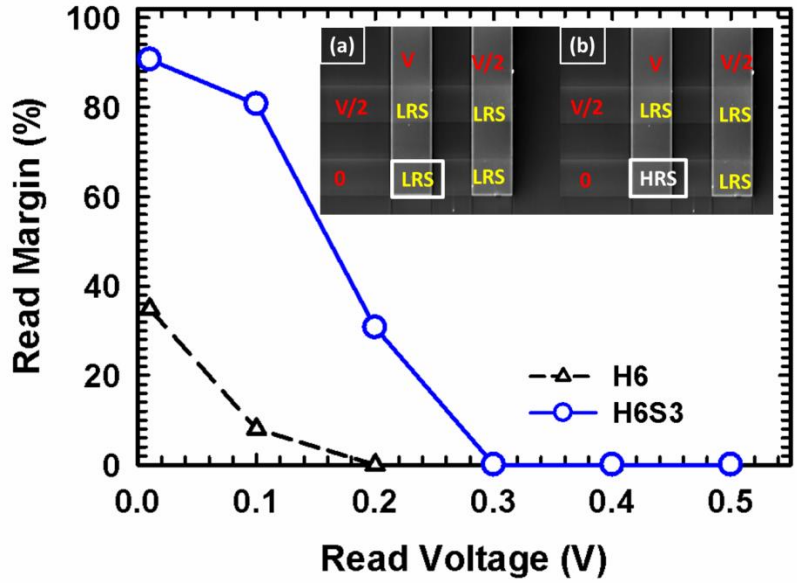


Figure 6.5. Experimental results of read margin as a function of read voltage on H6 and H6S3 devices.

## 6.4 CONCLUSION

In conclusion, the intrinsic nonlinear characteristics have been realized in the bilayer selectorless 1R-only RRAM without an additional transistor or a selector integration. The bilayer selectorless RRAM have been demonstrated by utilizing the intrinsic nonlinear characteristics without additional selector integration. The bilayer structures i.e. high-k layer/low-k layer stacks are highly scalable, while suppressing the sneak path currents and reading error in crossbar RRAM array. In this chapter, the numerical read margin calculated results provide additional insights and predictions into development bilayer selectorless RRAM array i.e. $HfO_x$ (7 nm) /graphite (5 nm) with high nonlinearity (~120), good memory window (~$10^2$), large array size (N~120) on the premise of 10% read margin, and low switching energy (~40 pJ/bit), which enable the low-power crossbar array memory applications.

# Future Work

First, the reliability properties of selectorless RRAM in relation of read margin changes i.e. the degradation of nonlinearity is proposed for future work. The mechanism understanding and potential modeling will provide the guidance towards the selectorless RRAM array design. The failure mechanism understanding is important before the selectorless RRAM cell can be successfully applied in the crossbar configurations.

Second, the readout circuit design for selectorless RRAM crossbar array is proposed and become important in order to realize the different writing schemes as well as sensing schemes. In addition, the sneak path current cancellation approaches applied on different high-k/low-k bilayer stacked selectorless RRAMs is worthy for further development.

Finally, the "multi-functional seletorless RRAM" is also proposed for future work, this is expected to show the volatile and non-volatile switching behaviors while demonstrating the synaptic behaviors[143-145] (e.g. long-term potentiation and long-term depression). The mechanism understanding and modeling are proposed, in which the thermal and electrical factors are suggested to be considered. The flexibility of multi-functional selectorless RRAM is proposed as one of the future research directions, which aims to the neuromorphic computing and high-density memory storage applications.

# Appendix A

Journal Papers:


[1] **Ying-Chen Chen**, Hui-Chun Huang, Chih-Yang Lin, Szu-Tung Hu, Yao-Feng Chang and Jack C. Lee "Selectorless Resistive Switching Memory: Non-uniform Dielectric Architecture and Seasoning Effect Determination for Low Power Array Applications", AIP Advances (2019)

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## Conference papers:

[1] **Ying-Chen Chen**, Chao-Cheng Lin, Sungjun Kim, and Jack C. Lee, "Selectorless Oxide-based Resistive Switching Memory with Nonuniform Dielectric for Low Power Crossbar Array Applications" ECS Transactions (2019)

[2] **Ying-Chen Chen**, Szu-Tung Hu, Chao-Cheng Lin, Jack C. Lee, "Resistive Switching Early Failure and Gap Identification in Bilayer Selectorless RRAM Applications" 77th Device Research Conference (DRC) (2019)

[3] **Y. -C. Chen**, C. -Y. Lin, H. -C. Huang and J. C. Lee "Energy Efficient Operation Schemes of Nonlinear Selectorless RRAM for Crossbar Array Applications" 61st Electronic Materials Conference (EMC) (2019)

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[5] **Ying-Chen Chen**, Xiaohan Wu, Yao-Feng Chang and Jack C. Lee, "Nonlinearity Enhancement by Positive Pulse Stress in Multilevel Cell Selectorless RRAM Applications" Device Research

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